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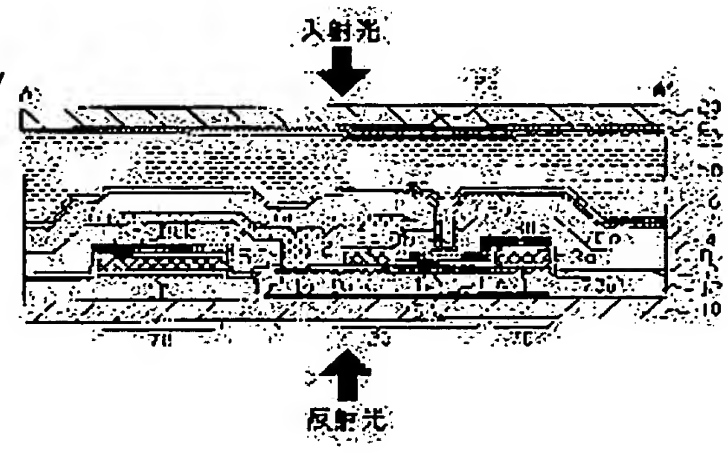
(54) ELECTRO-OPTIC DEVICE, METHOD OF MANUFACTURING THE SAME AND ELECTRONIC APPLIANCE

(57)Abstract:
PROBLEM TO BE SOLVED: To increase the pixel opening rate while connecting a pixel electrode to a semiconductor layer and to make high-quality image display possible in a rather simple structure in an electro-optic device using a TFT active matrix driving system.
SOLUTION: The pixel electrode and the TFT are connected by way of a first barrier layer 80a through a contact hole 8a and a contact hole 8b. A second barrier layer 80b is formed wider than a data line 6a, and one end of the layer 80b is overlapped on the pixel electrode 9a to determine the pixel opening region.



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CLAIMS

[Claim(s)]
[Claim 1] The thin film transistor and pixel electrode which have been arranged at the substrate corresponding to the crossover of two or more scanning lines, two or more data lines, and the said each scanning line and said each data line, The 1st conductive layer of the protection-from-light nature which intervened between the semi-conductor layer which constitutes the source and the drain field of said thin film transistor, and said pixel electrode, was electrically connected with said semi-conductor layer, and was electrically connected with said pixel electrode, The electro-optic device characterized by having the 2nd conductive layer which consisted of the same film as said 1st conductive layer, saw superficially, and has lapped with said data line partially at least.

[Claim 2] Said 2nd conductive layer is an electro-optic device according to claim 1 characterized by having seen superficially and having lapped with said pixel electrode partially at least.
[Claim 3] Said 1st conductive layer is an electro-optic device according to claim 1 or 2 characterized by having connected electrically through said semi-conductor layer and 1st contact hole, and connecting electrically through said pixel electrode and 2nd contact hole.
[Claim 4] Said data line is an electro-optic device given in any 1 term of claims 1-3 characterized by connecting electrically through said semi-conductor layer and 3rd contact hole.
[Claim 5] Said data line is an electro-optic device given in any 1 term of claims 1-4 characterized by seeing superficially and not lapping with said pixel electrode partially at least.
[Claim 6] Said 2nd conductive layer is an electro-optic device given in any 1 term of claims 1-5 characterized by connecting with a constant potential line electrically.
[Claim 7] An electro-optic device given in any 1 term of claims 1-6 characterized by having further the light-shielding film formed in said substrate side of a channel field through the substrate insulator layer at least among said semi-conductor layers.
[Claim 8] For said 1st conductive layer and said 2nd conductive layer, claims 1-7 characterized by including a refractory metal are electro-optic devices given in **** either.
[Claim 9] Said 2nd conductive layer and said data line are an electro-optic device given in any 1 term of claims 1-8 characterized by carrying out opposite arrangement partially at least through an interlayer insulation film.
[Claim 10] An electro-optic device given in any 1 term of claims 1-9 characterized by having further the storage capacitance connected to said pixel electrode.
[Claim 11] Said 1st conductive layer and said 2nd conductive layer are an electro-optic device according to claim 10 characterized by being prepared through an insulator layer on one electrode of said scanning line and said storage capacitance.
[Claim 12] The electro-optic device according to claim 11 which opposite arrangement of the 1st storage capacitance electrode which consists of said a part of semi-conductor layer, and the 2nd storage capacitance electrode which is one electrode of said storage capacitance is carried out through the 1st dielectric film, and is characterized by carrying out opposite arrangement of the 3rd storage capacitance electrode which consists of a part of said 2nd storage capacitance electrode and said 1st conductive layer through the 2nd dielectric film, and forming said storage capacitance.
[Claim 13] Said 2nd conductive layer is an electro-optic device given in any 1 term of claims 10-12 characterized by connecting with said 2nd storage capacitance electrode.
[Claim 14] It is the electro-optic device according to claim 13 which said 2nd conductive layer is electrically

connected to said 2nd storage capacitance electrode through the 4th contact hole, and is characterized by said 4th contact hole being punctured by the same process as the process which punctures said 1st contact hole.
[Claim 15] Said 2nd storage capacitance electrode is an electro-optic device according to claim 12 which is installed and is characterized by being a capacity line.
[Claim 16] Said 2nd storage capacitance electrode is an electro-optic device according to claim 13 characterized by coming to connect with said light-shielding film.
[Claim 17] Said light-shielding film is an electro-optic device according to claim 16 which serves as a capacity line and is characterized by coming to connect it with said light-shielding film while said 2nd storage capacitance electrode is constituted in the shape of an island for every elongation and pixel electrode along with said scanning line in between the data lines with which the flat-surface configuration on said substrate adjoins each other.
[Claim 18] For said 4th contact hole, said light-shielding film is an electro-optic device according to claim 15 characterized by connecting with said capacity line electrically through the 5th contact hole punctured by different flat-surface location.
[Claim 19] Said 2nd conductive layer and said light-shielding film are an electro-optic device given in any 1 term of claims 10-18 which it comes to connect electrically through said 2nd storage capacitance electrode, and are characterized by coming to connect said 2nd conductive layer and said light-shielding film with an adjoining pixel electrode.
[Claim 20] Said 1st conductive layer and said 2nd conductive layer are an electro-optic device given in any 1 term of claims 1-19 characterized by being prepared in the lower layer rather than said data line.
[Claim 21] Said 2nd conductive layer is an electro-optic device given in any 1 term of ****** 1-20 characterized by specifying partially at least the field which sees superficially, is prepared in the shape of an island, and met said data line among pixel opening fields.
[Claim 22] Said 1st conductive layer and said 2nd conductive layer are an electro-optic device given in any 1 term of claims 1-10 characterized by being prepared in the upper layer rather than said data line.
[Claim 23] Said 2nd conductive layer is an electro-optic device according to claim 22 characterized by specifying the field which is prepared in the shape of a grid except for the field where it sees superficially and said 1st conductive layer exists, and met said data line and said scanning line of a pixel opening field.
[Claim 24] Said semi-conductor layer and said 1st conductive layer are an electro-optic device according to claim 22 or 23 characterized by connecting through the junction conductive layer which consists of the same film as said data line.
[Claim 25] It is the electro-optic device according to claim 24 which has the storage capacitance connected to said pixel electrode, and is characterized by ****(ing) said data line through an interlayer insulation film between one electrode of said storage capacitance, and said 2nd conductive layer.
[Claim 26] In the manufacture approach of an electro-optic device of having the pixel electrode by which the thin film transistor connected to the scanning line, two or more data lines, and two or more of said each scanning line and said each data line and said thin film transistor were connected to the substrate The process which forms the semi-conductor layer used as a source field, a channel field, and a drain field in said substrate, The process which forms an insulating thin film on said semi-conductor layer, and the process which forms one electrode of the scanning line and storage capacitance on said insulating thin film, The process which forms the 1st interlayer insulation film on said scanning line and one [said] electrode, The process which punctures the 1st contact hole which leads to said semi-conductor layer to said insulating thin film and said 1st interlayer insulation film, The process which forms the 2nd conductive layer from the same film as the 1st conductive layer of protection-from-light nature, and said 1st conductive layer so that it may connect with said semi-conductor layer electrically through said 1st contact hole on said 1st interlayer insulation film, The process which forms the 2nd interlayer insulation film on said 1st conductive layer and said 2nd conductive layer, The process which forms the data line on said 2nd interlayer insulation film, and the process which forms the 3rd interlayer insulation film on said data line, The process which punctures the 2nd contact hole which leads to said 2nd interlayer insulation film and said 3rd interlayer insulation film at said 1st conductive layer, It is the manufacture approach of the electro-optic device characterized by being formed so that it may have the process which forms a pixel electrode so that it may connect with said 1st conductive layer electrically through said 2nd contact hole, and said 2nd conductive layer may be seen superficially and it may lap with said data line partially at least.

[Claim 27] In the process which forms said data line after the process which forms said 2nd interlayer insulation film, including further the process which punctures the 3rd contact hole which leads to said semi-conductor layer to said 2nd interlayer insulation film In the process which forms said data line so that it may connect with said semi-conductor layer electrically through said 3rd contact hole, and punctures said 1st contact hole In the process which punctures the 4th contact hole which leads to one electrode of said storage capacitance to said 1st interlayer insulation film at the same time it punctures said 1st contact hole, and forms said 2nd conductive layer The manufacture approach of the electro-optic device according to claim 23 characterized by forming said 2nd conductive layer so that it may connect with one electrode of said storage capacitance electrically through said 4th contact hole.

[Claim 28] In the manufacture approach of an electro-optic device of having the pixel electrode by which the thin film transistor connected to the scanning line, two or more data lines, and two or more of said each scanning line and said each data line and said thin film transistor were connected to the substrate The process which forms the semi-conductor layer used as a source field, a channel field, and a drain field in said substrate, The process which forms an insulating thin film on said semi-conductor layer, and the process which forms one electrode of the scanning line and storage capacitance on said insulating thin film, The process which forms the 1st interlayer insulation film on one electrode of said scanning line and storage capacitance, The process which punctures the 1st contact hole which leads to said semi-conductor layer to said 1st interlayer insulation film, The process which forms a junction conductive layer from the same film as said data line so that it may connect with said semi-conductor layer electrically through said 1st contact hole at the same time it forms the data line on said 1st interlayer insulation film, The process which forms the 2nd interlayer insulation film on said data line and said junction conductive layer, The process which punctures the 2nd contact hole which leads to said 2nd layer insulation gland at said junction conductive layer, At the same time it forms the 1st conductive layer of protection-from-light nature so that it may connect with said junction conductive layer electrically through said 2nd contact hole on said 2nd interlayer insulation film The process which forms the 2nd conductive layer which consists of the same film as said 1st conductive layer so that it may lap with said data line superficially, The process which forms the 3rd interlayer insulation film on said 1st conductive layer and said 2nd conductive layer, The manufacture approach of the electro-optic device characterized by including the process which punctures the 3rd contact hole which leads to said 3rd interlayer insulation film at said 1st conductive layer, and the process which forms a pixel electrode so that it may connect electrically through said 3rd contact hole at said 1st conductive layer.

[Claim 29] In the process which forms said data line after the process which forms said 1st interlayer insulation film, including further the process which punctures the 4th contact hole which leads to said semi-conductor layer to said 1st interlayer insulation film In the process which forms said data line so that it may connect with said semi-conductor layer electrically through said 4th contact hole, and punctures said 2nd contact hole In the process which punctures the 5th contact hole which leads to one electrode of said storage capacitance at said 1st interlayer insulation film and said 2nd layer insulation gland at the same time it punctures said 2nd contact hole, and forms said 2nd conductive layer The manufacture approach of the electro-optic device according to claim 24 characterized by forming said 2nd conductive layer so that it may connect with one electrode of said storage capacitance electrically through said 5th contact hole.

[Claim 30] Electronic equipment characterized by having the electro-optic device of a publication in any 1 term of claim 1 to claim 25.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention belongs to the technical field of an electro-optic device and its manufacture approach, and belongs to an electro-optic device equipped with the conductive layer for the junction for taking an electric flow good especially between a pixel electrode and the thin film transistor for pixel switching (TFT being called suitably below Thin Film Transistor), and its manufacture approach list at the technical field of electronic equipment.
[0002]
[Description of the Prior Art] Conventionally, come to **** electrooptic material, such as liquid crystal, between the substrates of a pair, and this kind of electro-optic device to the TFT array substrate which is an example of one substrate Two or more pixel electrodes are prepared in the shape of a matrix, and to the opposite substrate which is an example of the substrate of another side In order to specify the pixel opening field (namely, field where light passes the electrooptic material part in each pixel) in each pixel, it is common that a light-shielding film is prepared in the shape of a grid corresponding to the gap of a pixel electrode. In this case, in order to make it the contrast ratio in a display image not fall by optical leakage around each pixel electrode, it is constituted so that it may see superficially and a grid-like light-shielding film may lap with each pixel electrode a little. Under the present circumstances, since especially the light-shielding film prepared in the opposite substrate side is comparatively separated from the pixel electrode through electrooptic material etc., in consideration of the lamination gap of light and both substrates which carries out incidence, it is necessary to put it aslant by the margin with remarkable pixel electrode and light-shielding film like ****. This serves as a big obstruction at the time of raising a pixel numerical aperture (namely, rate which the pixel opening field in each pixel occupies).
[0003] So, recently, under the general request of performing bright image display, in order to raise the pixel numerical aperture in each pixel, the technique of specifying each pixel opening field partially is also generalized by only the protection-from-light gland by the side of an opposite substrate not prescribing a pixel opening field, but forming the data line broadly so that the clearance between the lengthwise directions of a pixel electrode may be covered from protection-from-light nature ingredients, such as aluminum (aluminum). According to this technique, since the data line prescribed the pixel opening field partially, a pixel numerical aperture can be raised.
[0004] On the other hand, in this kind of electro-optic device, although it is necessary to connect mutually, each pixel electrode and switching elements, such as TFT prepared for example, in each pixel Since two or more interlayer insulation films for insulating electrically wiring and these of the scanning line, a capacity line, the data line, etc. mutually are included, for example, 1000nm (nano meter) extent or a thicker laminated structure than it exists among both, It becomes difficult to puncture the contact hole for connecting between both electrically.
[0005] Under a general request called high-definition-izing of the display image in this kind of electro-optic device, improvement in detailed-izing of a pixel pitch and a pixel numerical aperture, adequate supply of the picture signal to a pixel electrode, etc. become important.
[0006] However, since the data line and a pixel electrode have lapped partially through the interlayer insulation film according to the technique of specifying a pixel opening field partially with the data line mentioned above, if TFT prepared in each pixel is considered, according to the lap of the data line and the pixel electrode which

were mentioned above, parasitic capacitance will arise between the source and a drain. Switching operation is carried out so that TFT to which a picture signal is supplied through the data line generally [here] may make the fixed potential according to a picture signal hold to a pixel electrode for an one-frame period, but during this period, since it sways frequently to the potential of the picture signal supplied to TFT of an other bank, the electrical potential difference which TFT should carry out [an electrical potential difference] abnormality actuation and should be made to hold to a pixel electrode will leak the data line with the parasitic capacitance between the above-mentioned source and a drain. Consequently, supply of the picture signal to a pixel electrode becomes unstable, and while saying that degradation of a display image is finally caused, there is ****.

[0007] On the other hand, under a general request called the simplification and low-cost-izing of an equipment configuration in this kind of electro-optic device, also in case a certain function is added or raised, it becomes important to use effectively not to make the conductive layer in a laminated structure or the number of insulator layers increase recklessly or one film in order to achieve two or more set ability.

[0008] This invention is made in view of an above-mentioned trouble, and it has the comparatively easy configuration, and a pixel numerical aperture is high and let it be a technical problem to offer the high-definition electro-optic device in which image display is possible and its high-definition manufacture approach.

[0009]

[Means for Solving the Problem] In order that the electro-optic device of this invention may solve the above-mentioned technical problem, to a substrate Two or more scanning lines, The thin film transistor and pixel electrode which have been arranged corresponding to the crossover of two or more data lines, and the said each scanning line and said each data line, The 1st conductive layer of the protection-from-light nature which intervened between the semi-conductor layer which constitutes the source and the drain field of said thin film transistor, and said pixel electrode, was electrically connected with said semi-conductor layer, and was electrically connected with said pixel electrode, It consists of the same film as said 1st conductive layer, and has the 2nd conductive layer which saw superficially and has lapped with said data line partially at least.

[0010] According to the configuration of the electro-optic device of this invention, it intervenes between a semi-conductor layer and a pixel electrode, and connects with the semi-conductor layer electrically by one side, and the 1st conductive layer is another side and is electrically connected with the pixel electrode. Therefore, the 1st conductive layer becomes possible [avoiding the difficulty in the case of functioning as a conductive layer for the junction for connecting electrically a pixel electrode and the drain field of a semi-conductor layer, for example, carrying out direct continuation of between both through one contact hole].

[0011] Moreover, since the 2nd conductive layer was seen superficially and has lapped with said data line partially at least, it becomes possible [carrying out the redundancy of the protection from light of each pixel by the 2nd conductive layer in addition to the data line].

[0012] In the mode of 1 of the electro-optic device of this invention, said 2nd conductive layer was seen superficially and has lapped with said pixel electrode partially at least.

[0013] According to this configuration, especially the 2nd conductive layer formed between the pixel electrodes which see superficially and adjoin partially at least has lapped with the pixel electrode. For this reason, the 2nd conductive layer part which lapped with this pixel electrode and a partial target can prescribe the pixel opening field in each pixel partially at least. Under the present circumstances, especially in the part where the pixel opening field was specified by the 2nd conductive layer, since it sees superficially and there is no clearance between a pixel electrode and the 2nd conductive layer, the optical leakage through such a clearance does not take place. Consequently, finally a contrast ratio is raised. Since the data line does not need to prescribe a pixel opening field like before, it becomes unnecessary to pile up the data line and a pixel electrode in the part where the pixel opening field was specified to coincidence by the 2nd conductive layer. Consequently, it is not necessary to generate the parasitic capacitance between the sources of a thin film transistor and the drains in each pixel according to the structure where the data line and a pixel electrode lap through an interlayer insulation film. For this reason, it originates in the potential shake concerned of the data line which sways frequently to the potential of the picture signal supplied in predetermined periods, such as one etc. frame, at the thin film transistor of an other bank, a thin film transistor carries out abnormality actuation with the parasitic capacitance between the above-mentioned source and a drain, and the situation which the electrical potential difference which should be made to hold to a pixel electrode leaks can be prevented. That is, switching operation of the thin film transistor is carried out, it can supply a picture signal adequately to a pixel electrode

through the data line and a thin film transistor, and, finally high definition-ization of a display image of it is attained by reduction of a flicker or line nonuniformity so that the fixed potential according to a picture signal may be made to hold to a pixel electrode.

[0014] Furthermore, since the function to specify a pixel opening field is given closing adequate supply of a picture signal to it if to the 2nd conductive layer which consists of the same film as this 1st conductive layer while giving the function to relay a thin film transistor and a pixel electrode to the 1st conductive layer, low cost-ization can be attained in the simplification list of a laminated structure and a manufacture process as a whole.

[0015] In other modes of the electro-optic device of this invention, it connects electrically through said semi-conductor layer and 1st contact hole, and said 1st conductive layer is electrically connected through said pixel electrode and 2nd contact hole.

[0016] According to this configuration, as compared with the case where one contact hole is punctured, the path of a contact hole can be made small from a pixel electrode to the drain field of a semi-conductor layer. That is, in order that etching precision may fall, in order to prevent the thrust omission in a thin semi-conductor layer, the dry etching which can make the path of a contact hole small must be stopped on the way, a process must be constructed so that it may finally puncture to a semi-conductor layer by wet etching, and the path of a contact hole cannot but spread by wet etching without directivity, so that a contact hole is generally punctured deeply. On the other hand, in this mode, since what is necessary is just to connect between semi-conductor layers with a pixel electrode by the 1st and 2nd two in-series contact holes, it becomes possible to shorten distance which becomes possible [puncturing each contact hole by dry etching], or is punctured by wet etching at least. Consequently, the path of each contact hole can be made small, respectively, and flattening in the pixel electrode section located above the 1st or 2nd contact hole is promoted.

[0017] According to other modes of the electro-optic device of this invention, said data line is electrically connected through said semi-conductor layer and 3rd contact hole.

[0018] According to this configuration, the electric connection between the data line and the source field of a semi-conductor layer is obtained good through the 3rd contact hole.

[0019] According to other modes of the electro-optic device of this invention, said data line is seen superficially and does not lap with said pixel electrode partially at least.

[0020] According to this configuration, by forming so that the data line and a pixel electrode may not lap as much as possible, it compares with the case where the data line and a pixel electrode are piled up, and the parasitic capacitance between the data line and a pixel electrode can be reduced certainly. Therefore, the electrical potential difference especially in a pixel electrode is stabilized, and a flicker and line nonuniformity can be reduced.

[0021] furthermore, the part with which the data line and a pixel electrode lapped through the interlayer insulation film -- it is and electric [between both with high possibility of generating] -- generating of defects, such as being short (short circuit), can be suppressed, and, finally decline in the rate of an equipment defect and improvement in the yield at the time of manufacture are achieved.

[0022] Other mode ****** of the electro-optic device of this invention and said 2nd conductive layer are electrically connected to the constant potential line.

[0023] According to this configuration, some parasitic capacitance is attached between the pixel electrode and the 2nd conductive layer which have lapped with the part at least, but the potential of the 2nd conductive layer is maintained at constant potential. for this reason, the bad influence which potential fluctuation of the 2nd conductive layer has on the potential of a pixel electrode through the parasitic capacitance between a pixel electrode and the 2nd conductive layer -- it can decrease -- a pixel electrode -- the electrical potential difference to kick is stabilized more and a flicker and line nonuniformity can be reduced further.

[0024] According to other modes of the electro-optic device of this invention, it has further the light-shielding film formed in said substrate side of a channel field through the substrate insulator layer at least among said semi-conductor layers.

[0025] According to this configuration, the channel field to the light from a TFT array substrate side can be shaded by the light-shielding film formed in the substrate side of a channel field through the substrate insulator layer at least among semi-conductor layers. For this reason, high-definition image display becomes possible, reducing the optical leak in a channel field which originates in the optical exposure to thin film transistors, such

as incident light, the rear-face reflected light, and the reflected light, and is generated at the time of actuation of the electro-optic device concerned, and reducing property change and degradation of a thin film transistor.
[0026] According to other modes of the electro-optic device of this invention, said 1st conductive layer and said 2nd conductive layer contain a refractory metal.
[0027] according to this configuration -- ******** and an arrow -- two conductive layer consists of the metal simple substance containing at least one of Ti (titanium), Cr (chromium), W (tungsten), Ta (tantalum), Mo (molybdenum), and Pb(s) (lead), an alloy, metal silicide, etc. For this reason, by high temperature processing in the various processes performed after the 1st conductive layer and the 2nd conductive layer formation in a manufacture process, the 1st conductive layer and the 2nd conductive layer concerned deform, or do not break.
[0028] According to other modes of the electro-optic device of this invention, opposite arrangement of said 2nd conductive layer and said data line is partially carried out at least through an interlayer insulation film.
[0029] according to this configuration, but [not between the pixel electrodes with which potential is changed according to the picture signal which should be held] between the 2nd conductive layer by which potential was stabilized more, since capacity is added to the data line, it is possible to make it increase moderately, making it not cause the potential shake of the data line -- HI -- ** Even if it makes especially a pixel pitch detailed and makes data-line width of face detailed in connection with this, by making the capacity between the 2nd conductive layer increase, the lack of capacity of the data line can be suppressed and the write-in deficiency in performance in supply to the pixel electrode of the picture signal through the data line concerned can be prevented.
[0030] According to other modes of the electro-optic device of this invention, it has further the storage capacitance connected to said pixel electrode.
[0031] According to this configuration, the electrical-potential-difference holding time of the picture signal in a pixel electrode can be lengthened far, and storage capacitance raises a contrast ratio very efficiently.
[0032] In this mode, said 1st conductive layer and 2nd conductive layer may be prepared through an insulator layer on one electrode of said scanning line and said storage capacitance.
[0033] According to this configuration, by the 2nd conductive layer possible [a pixel electrode and a semi-conductor layer] and prepared through the insulator layer on one electrode of the scanning line and storage capacitance, the 1st conductive layer prepared through the insulator layer on one electrode of the scanning line and storage capacitance can prescribe a pixel opening field, and a configuration becomes possible simply about capacity between the 2nd conductive layer and one electrode of storage capacitance further.
[0034] In the mode further equipped with this storage capacitance, opposite arrangement of the 1st storage capacitance electrode which consists of said a part of semi-conductor layer, and the 2nd storage capacitance electrode which is one electrode of said storage capacitance is carried out through the 1st dielectric film, opposite arrangement of the 3rd storage capacitance electrode which consists of a part of said 2nd storage capacitance electrode and said 1st conductive layer may be carried out through the 2nd dielectric film which is said insulator layer, and said storage capacitance may be formed.
[0035] According to this configuration, opposite arrangement of the 1st storage capacitance electrode which consists of a part of semi-conductor layer, and the 2nd storage capacitance electrode which is one electrode of storage capacitance is carried out through the 1st dielectric film, the 1st storage capacitance is constituted, opposite arrangement of the 3rd storage capacitance electrode which consists of a part of 2nd storage capacitance electrode and 1st conductive layer is carried out through the 2nd dielectric film on the other hand, and the 2nd storage capacitance is constituted. And since storage capacitance is formed in each pixel electrode from these 1st and 2nd storage capacitance, a non-pixel opening field is used effectively and, moreover, comparatively mass storage capacitance can be built using three-dimensional structure.
[0036] Said 2nd conductive layer may be connected to said 2nd storage capacitance electrode in the mode further equipped with this storage capacitance.
[0037] According to this configuration, some parasitic capacitance is attached between the pixel electrode and the 2nd conductive layer which have lapped partially at least, but the potential of the 2nd conductive layer is maintained at the potential of the 2nd storage capacitance electrode.
[0038] Thus, when connecting the 2nd conductive layer to the 2nd storage capacitance electrode, said 2nd conductive layer is connected to said 2nd storage capacitance electrode through the 4th contact hole, and said 4th contact hole may be punctured by the same process as the process which punctures said 1st contact hole.

[0039] According to this configuration, since the 2nd conductive layer can be connected to the 2nd storage capacitance electrode comparatively easily and the 4th contact hole is punctured to puncturing the 1st contact hole moreover and coincidence, it is useful to the simplification of a manufacture process.
[0040] The 2nd storage capacitance electrode here is built and is good also as a capacity line.
[0041] According to this configuration, a capacity line is made into constant potential, or it is large capacity at least, and that potential fluctuation is small. For this reason, the bad influence which potential fluctuation of the 2nd conductive layer has on the potential of a pixel electrode can be reduced through the parasitic capacitance between a pixel electrode and the 2nd conductive layer.
[0042] This 2nd storage capacitance electrode may be connected with ******.
[0043] According to this configuration, potential of the 2nd storage capacitance electrode and a light-shielding film can be made the same, and if the configuration which makes predetermined potential either the 2nd storage capacitance electrode and protection-from-light gland is taken, potential of another side will also be made with predetermined potential. Consequently, the bad influence by the potential shake in the 2nd storage capacitance electrode or a light-shielding film can be reduced. Moreover, wiring and the capacity line which consist of a light-shielding film can be mutually operated as redundancy wiring.
[0044] This light-shielding film serves as a capacity line, and said 2nd storage capacitance electrode may be connected to said light-shielding film while it is constituted in the shape of an island for every elongation and pixel electrode along with said scanning line in between the data lines with which the flat-surface configuration on said substrate adjoins each other.
[0045] According to this configuration, since the 2nd storage capacitance electrode can be constituted in the shape of an island for every pixel electrode, a pixel numerical aperture can be raised. Moreover, the 2nd storage capacitance can also be made redundancy wiring of a capacity line with wiring, then a light-shielding film.
[0046] Furthermore, said light-shielding film may be electrically connected to said capacity line through the 5th contact hole punctured by different flat-surface location from said 4th contact hole.
[0047] According to this configuration, the channel field to the light from a substrate side can be shaded by the light-shielding film formed in the substrate side of a channel field through the substrate insulator layer at least among semi-conductor layers. And a light-shielding film is conductivity, and since it connects with the capacity line through the 5th contact hole, it becomes possible to operate a light-shielding film of it as redundancy wiring of a capacity line, and, finally it can attain high definition-ization of a display image by stabilizing the potential of a capacity line more by attaining low resistance-ization of a capacity line. Moreover, the 4th contact hole and the 5th contact hole can prevent the faulty connection in the 4th contact hole and the 5th contact hole by forming in a different flat-surface location.
[0048] Furthermore, it may come to connect said 2nd conductive layer and said light-shielding film electrically through said 2nd storage capacitance electrode, and said 2nd conductive layer and said light-shielding film may be connected to the adjoining pixel electrode.
[0049] According to this configuration, the 2nd conductive layer can be used as a capacity line. Moreover, by making the 2nd storage capacitance electrode into a capacity line, and connecting the 2nd conductive layer and the 2nd storage capacitance electrode, it can be double, a capacity line can be formed and redundant structure can be realized.
[0050] According to other modes of the electro-optic device of this invention, said 1st conductive layer and said 2nd conductive layer are prepared in the lower layer rather than said data line.
[0051] According to this configuration, by the 2nd conductive layer possible [a pixel electrode and a semi-conductor layer] and prepared in the lower layer rather than the data line, the 1st conductive layer prepared in the lower layer can prescribe a pixel opening field, and a configuration becomes possible from the data line simply about capacity between the 1st conductive layer and the 2nd storage capacitance electrode further.
[0052] According to other modes of the electro-optic device of this invention, said 2nd conductive layer is seen superficially, is prepared in the shape of an island, and specifies partially at least the field which met said data line among pixel opening fields.
[0053] According to this configuration, the 2nd conductive layer which saw superficially and was prepared in the shape of an island can prescribe partially at least the field which met the data line among pixel opening fields. For example, the 2nd conductive layer can be formed in the field of most except the field where the contact hole which connects the channel field, the data line, and the semi-conductor layer of a thin film

transistor among the pixel opening fields which met the data line was punctured, and it is possible to specify the pixel opening field in the field of this most by the 2nd conductive layer concerned.
[0054] Or according to other modes of the electro-optic device of this invention, said 1st conductive layer and said 2nd conductive layer are characterized by being prepared as a layer further than said data line from said substrate (i.e., the upper layer).
[0055] According to this configuration, the 2nd conductive layer which junction of a pixel electrode and a semi-conductor layer is possible, and was prepared in the upper layer rather than the data line by the 1st conductive layer prepared as a layer further than the data line from a substrate can prescribe a pixel opening field. In this case, especially, the 2nd conductive layer may be prepared in all the fields on the data line through an interlayer insulation film, and may be prepared through an interlayer insulation film on the scanning line. Moreover, since the location of the contact hole which connects the 1st conductive layer and a pixel electrode can be set as the location of arbitration if it is in a non-opening field, it increases [a design degree of freedom] and is advantageous.
[0056] Said 2nd conductive layer is prepared in the shape of [said] a grid except for the field where it sees superficially and said 1st conductive layer exists, and it may consist of this mode so that the field which met said data line and said scanning line of a pixel opening field, respectively may be specified.
[0057] According to this configuration, since it is prepared in the shape of a grid except for the field where the 1st conductive layer exists, the 2nd conductive layer can specify the field met, respectively to the data line and the scanning line of a pixel opening field, i.e., also specify all the profiles of a pixel opening field. In addition, about the gap of the 1st conductive layer and the 2nd conductive layer, optical leakage can be easily prevented by the light-shielding film by the side of an opposite substrate, the thin film transistor of the thin film transistor bottom, the installation part of the data line, etc., for example.
[0058] In the mode by which this 1st conductive layer and 2nd conductive layer were prepared in the upper layer, said semi-conductor layer and said 1st conductive layer may be connected through the junction conductive layer which consists of the same film as said data line.
[0059] Since according to this configuration from a pixel electrode to the junction conductive layer which consists of the same layer as the data line is connected electrically and even the semi-conductor layer was further connected electrically by this junction conductive layer rather than the data line by the 1st conductive layer prepared in the upper layer, junction becomes possible good about from a pixel electrode to a semi-conductor layer by the 1st conductive layer and junction conductive layer which are two conductive layers for junction. Also when the electric affinity of aluminum film which constitutes especially the data line, and the ITO (Indium Tin Oxide) film which constitutes a pixel electrode is bad, it is advantageous at the point which should just form the 1st conductive layer from a congenial ingredient (for example, refractory metal) electrically with these both.
[0060] In the mode by which this 1st conductive layer and 2nd conductive layer are prepared in the upper layer, it has the storage capacitance connected to said pixel electrode, and said data line may be ****(ed) through an interlayer insulation film between one electrode of said storage capacitance, and said 2nd conductive layer.
[0061] According to this configuration, but [not between the pixel electrodes with which potential is changed according to the picture signal which should be held] between one electrodes of the 2nd conductive layer by which potential was stabilized more, and storage capacitance, since capacity can be made to add to the data line, it becomes possible to make the capacity of the data line increase moderately, making it not cause a potential shake. Even if it makes especially a pixel pitch detailed and makes data-line width of face detailed in connection with this, by making the capacity between the 2nd conductive layer and the 2nd storage capacitance electrode increase, the lack of capacity of the data line can be suppressed and the write-in deficiency in performance in supply to the pixel electrode of the picture signal through the data line concerned can be prevented.
[0062] In order that the manufacture approach of the 1st electro-optic device of this invention may solve the above-mentioned technical problem In the manufacture approach of an electro-optic device of having the pixel electrode by which the thin film transistor connected to the scanning line, two or more data lines, and two or more of said each scanning line and said each data line and said thin film transistor were connected to the substrate The process which forms the semi-conductor layer used as a source field, a channel field, and a drain field in said substrate, The process which forms an insulating thin film on said semi-conductor layer, and the

process which forms one electrode of the scanning line and storage capacitance in the predetermined field on said insulating thin film, The process which forms the 1st interlayer insulation film on said scanning line and one [said] electrode, The process which punctures ** 1 contact hole which leads to said semi-conductor layer to said insulating thin film and said 1st interlayer insulation film, So that it may connect with said semi-conductor layer electrically through said 1st contact hole on said 2nd insulator layer The 1st conductive layer of protection-from-light nature, The process which forms the 2nd conductive layer from the same film as said 1st conductive layer, and the process which forms the 2nd interlayer insulation film on said 1st conductive layer and said 2nd conductive layer, The process which forms the data line on said 2nd **********, and the process which forms the 3rd interlayer insulation film on said data line, The process which punctures the 2nd contact hole which leads to said 2nd interlayer insulation film and said 3rd interlayer insulation film at said 1st conductive layer, It has the process which forms a pixel electrode so that it may connect with said 1st conductive layer electrically through said 2nd contact hole, and said 2nd conductive layer is formed so that it may see superficially and may lap with said data line partially at least.

[0063] According to the manufacture approach of the 1st electro-optic device of this invention, laminating formation of the 1st interlayer insulation film is carried out in this order in one electrode list of a semi-conductor layer, an insulating thin film, the scanning line, and storage capacitance at a substrate. Next, the 1st contact hole which leads to a semi-conductor layer is punctured by an insulating thin film and the 1st interlayer insulation film, and the 1st conductive layer of protection-from-light nature is formed so that it may connect with a semi-conductor layer electrically through this 1st contact hole. The 2nd conductive layer is formed so that it may be partially arranged at least in the gap of the field where it sees to coincidence superficially and a pixel electrode is formed in it from the same film as this 1st conductive layer. Then, laminating formation of the 2nd interlayer insulation film, the data line, and the 3rd interlayer insulation film is carried out in this order. Next, the 2nd contact hole which leads to the 1st conductive layer is punctured, and pixel ionization formation is carried out so that it may connect with the 1st conductive layer electrically through this 2nd contact hole. Therefore, the electro-optic device of this invention which has the configuration which forms the 1st and 2nd conductive layers as a layer near a substrate, and relays a pixel electrode and a semi-conductor layer by the 2nd conductive layer through two contact holes rather than the data line mentioned above can be manufactured comparatively easily. Since the 1st conductive layer and the 2nd conductive layer are especially formed from the same film, low cost-ization can be attained in the simplification list of a manufacture process.

[0064] In the mode of 1 of the manufacture approach of the 1st electro-optic device of this invention In the process which forms said data line after the process which forms said 2nd interlayer insulation film, including further the process which punctures the 3rd contact hole which leads to said semi-conductor layer to said 2nd interlayer insulation film In the process which forms said data line so that it may connect with said semi-conductor layer electrically through said 3rd contact hole, and punctures said 1st contact hole In the process which punctures the 4th contact hole which leads to one electrode of said storage capacitance to said 1st interlayer insulation film at the same time it punctures said 1st contact hole, and forms said 2nd conductive layer Said 2nd conductive layer is formed so that it may connect with one electrode of said storage capacitance electrically through said 4th contact hole.

[0065] According to this configuration, the 3rd contact hole which leads to a semi-conductor layer is punctured after formation of the 2nd interlayer insulation film, and the data line is formed so that it may connect with a semi-conductor layer electrically through this 3rd contact hole. Furthermore, the 4th contact hole which leads to one electrode of storage capacitance at coincidence is punctured at the time of puncturing of the 1st contact hole, and the 2nd conductive layer is formed so that it may connect with one electrode of storage capacitance electrically through this 4th contact hole. Therefore, the electro-optic device of this invention which has the configuration to which the data line and the semi-conductor layer which were mentioned above are electrically connected to through the contact hole, and the 2nd conductive layer and one electrode of storage capacitance were electrically connected through the contact hole can be manufactured comparatively easily. Since these two contact holes are especially punctured to coincidence, low cost-ization can be attained in the simplification list of a manufacture process.

[0066] In order that the manufacture approach of the 2nd electro-optic device of this invention may solve the above-mentioned technical problem In the manufacture approach of an electro-optic device of having the pixel electrode by which the thin film transistor connected to the scanning line, two or more data lines, and two or

more of said each scanning line and said each data line and said thin film transistor were connected to the substrate The process which forms the semi-conductor layer used as a source field, a channel field, and a drain field in said substrate, The process which forms an insulating thin film on said semi-conductor layer, and the process which forms one electrode of the scanning line and storage capacitance on said insulating thin film, The process which forms the 1st interlayer insulation film on one electrode of said scanning line and storage capacitance, The process which punctures the 1st contact hole which leads to said semi-conductor layer to said 1st interlayer insulation film, The process which forms a junction conductive layer from the same film as said data line so that it may connect with said semi-conductor layer electrically through said 1st contact hole at the same time it forms the data line on said 1st interlayer insulation film, The process which forms the 2nd interlayer insulation film on said data line and said junction conductive layer, The process which punctures the 2nd contact hole which leads to said 2nd interlayer insulation film at said junction conductive layer, At the same time it forms the 1st conductive layer of protection-from-light nature so that it may connect with said junction conductive layer electrically through said 2nd contact hole on said 2nd interlayer insulation film The process which forms the 2nd conductive layer which consists of the same film as said 1st conductive layer so that it may lap with said data line superficially, The process which forms the 3rd interlayer insulation film on said 1st conductive layer and said 2nd conductive layer, It is characterized by including the process which punctures the 3rd contact hole which leads to said 3rd interlayer insulation film at said 1st conductive layer, and the process which forms a pixel electrode so that it may connect electrically through said 3rd contact hole at said 1st conductive layer.

[0067] According to the manufacture approach of the 2nd electro-optic device of this invention, laminating formation of the 1st interlayer insulation film is carried out in this order in one electrode list of a semi-conductor layer, an insulating thin film, the scanning line, and storage capacitance at a substrate. Next, the contact hole which leads to a semi-conductor layer is punctured, and a junction conductive layer is formed from the same film as the data line so that it may connect with a semi-conductor layer electrically, at the same time the data line is formed. Next, after the 2nd interlayer insulation film is formed, the contact hole which leads to a junction conductive layer is punctured, and the 1st conductive layer of protection-from-light nature is formed so that it may connect with a junction conductive layer electrically. It can come, simultaneously the 2nd conductive layer is formed from the same film as the 1st conductive layer. Then, the 3rd interlayer insulation film is formed, the contact hole which leads to the 1st conductive layer is punctured, and a pixel electrode is formed so that it may connect with the 1st conductive layer electrically. Therefore, as the layer further than the data line from a substrate, i.e., the upper layer, while forming a junction conductive layer as a conductive layer which consists of the same film as the data line mentioned above, the 1st conductive layer is formed, and while relaying a pixel electrode and a semi-conductor layer by the junction conductive layer and the 1st conductive layer through three contact holes, the electro-optic device of this invention which has the configuration which specifies a pixel opening field by the 2nd conductive layer can be manufactured comparatively easily. Since the 1st conductive layer and the 2nd conductive layer are especially formed from the same film, low cost-ization can be attained in the simplification list of a manufacture process.

[0068] In the mode of 1 of the manufacture approach of the 2nd electro-optic device of this invention In the process which forms said data line after the process which forms said 1st interlayer insulation film, including further the process which punctures the 4th contact hole which leads to said semi-conductor layer to said 1st interlayer insulation film In the process which forms said data line so that it may connect with said semi-conductor layer electrically through said 4th contact hole, and punctures said 2nd contact hole In the process which punctures the 5th contact hole which leads to one electrode of said storage capacitance to said 1st interlayer insulation film and said 2nd interlayer insulation film at the same time it punctures said 2nd contact hole, and forms said 2nd conductive layer Said 2nd conductive layer is formed so that it may connect with one electrode of said storage capacitance electrically through said 5th contact hole.

[0069] According to this mode, the 4th contact hole which leads to a semi-conductor layer is punctured after formation of the 1st interlayer insulation film, and the data line is formed so that it may connect with a semi-conductor layer electrically. Furthermore, when puncturing a contact hole to the 2nd interlayer insulation film, the contact hole which leads to one electrode of storage capacitance at coincidence is punctured, and the 3rd conductive layer is formed so that it may connect with one electrode of storage capacitance electrically. Therefore, the electro-optic device of this invention which has the configuration to which the data line and the

semi-conductor layer which were mentioned above are electrically connected to through the contact hole, and the 2nd conductive layer and one electrode of storage capacitance were electrically connected through the contact hole can be manufactured comparatively easily. Since these two contact holes are especially punctured to coincidence, low cost-ization can be attained in the simplification list of a manufacture process.
[0070] Such an operation and other gains of this invention are made clear from the gestalt of the operation explained below.
[0071]
[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained based on a drawing.
[0072] (The 1st operation gestalt) The configuration of the electro-optic device in the 1st operation gestalt of this invention is explained with reference to drawing 4 from drawing 1 . Drawing 1 is equal circuits, such as various components in two or more pixels formed in the shape of [which constitutes the image display field of an electro-optic device] a matrix, and wiring, drawing 2 is a top view of two or more pixel groups where the TFT array substrate with which the data line, the scanning line, a pixel electrode, etc. were formed adjoins each other, drawing 3 is the A-A' sectional view of drawing 2 R> 2, and drawing 4 is B-B of drawing 2 , and a sectional view. In addition, in order to make each class and each part material into the magnitude of extent which can be recognized on a drawing, scales are made to have differed for each class or every each part material in drawing 3 and drawing 4 .
[0073] In drawing 1 , two or more formation of TFT30 for two or more pixels formed in the shape of [which constitutes the image display field of the electro-optic device in this operation gestalt] a matrix to control pixel electrode 9a corresponding to the crossover of scanning-line 3a and data-line 6a is carried out at the shape of a matrix, and data-line 6a to which a picture signal is supplied is electrically connected to the source concerned of TFT30. The picture signals Sl, S2, --, Sn written in data-line 6a may be supplied to line sequential, and you may make it supply them to this order for every group to two or more data-line 6a which adjoin each other. Moreover, scanning-line 3a is electrically connected to the gate of TFT30, and it consists of predetermined timing so that the scan signals Gl, G2, --, Gm may be impressed to scanning-line 3a in pulse line sequential at this order. It connects with the drain of TFT30 electrically, and pixel electrode 9a writes in the picture signals Sl and S2 supplied from data-line 6a in TFT30 which is a switching element when only a fixed period closes the switch, ---, and Sn to predetermined timing. Fixed period maintenance of the picture signals Sl, S2, --, Sn of the predetermined level written in liquid crystal as an example of electrooptic material through pixel electrode 9a is carried out between the counterelectrodes (it mentions later) formed in the opposite substrate (it mentions later). When the orientation and order of molecular association change with the voltage levels impressed, liquid crystal modulates light and enables a gradation display. According to the electrical potential difference impressed when it was in no MARI White mode, passage of this liquid crystal part of incident light is made impossible, if it is in NOMA reeve rack mode, according to the impressed electrical potential difference, passage of this liquid crystal part of incident light will be enabled, and light with the contrast according to a picture signal will carry out outgoing radiation from an electro-optic device as a whole. Here, storage capacitance 70 is added to the liquid crystal capacity and juxtaposition which are formed [that the held picture signal leaks and] between pixel electrode 9a and a counterelectrode at a **** sake. For example, as for the electrical potential difference of pixel electrode 9a, only time amount also with triple figures longer than the time amount to which the picture signal was impressed is held with storage capacitance 70 at the source of TFT30. Thereby, it is improved furthe and a maintenance property can realize the high electro-optic device of a contrast ratio.
[0074] In drawing 2 , on the TFT array substrate of an electro-optic device, two or more transparent pixel electrode 9a (the profile is shown by dotted-line section 9a') is prepared in the shape of a matrix, and data-line 6a, scanning-line 3a, and capacity line 3b are prepared respectively along the boundary of pixel electrode 9a in every direction. Data-line 6a is electrically connected to the below-mentioned source field through the contact hole 5 among semi-conductor layer 1a which a metaphor becomes from the polish recon film. Island-like 1st conductive layer (1st barrier layer is called hereafter) 80a and 2nd conductive layer (2nd barrier layer is called hereafter) 80b are prepared in the field (field shown with the slash of a drawing Nakamigi riser) in alignment with field and data-line 6a in alignment with scanning-line 3a in the gap between pixel electrode 9a which adjoin each other, respectively. Especially with this operation gestalt, 1st barrier layer 80a and 2nd barrier layer 80b are formed from the electric conduction film of the same protection-from-light nature. Pixel electrode 9a

relays 1st barrier layer 80a, and is electrically connected to the contact hole 8a list to the below-mentioned drain field among semi-conductor layer 1a through contact hole 8b. Capacity line 3b is electrically connected to 2nd barrier layer 80b through contact hole 8c. Moreover, scanning-line 3a is arranged so that the bottom of Fig. Nakamigi may counter channel field 1a' shown in the slash field of ** among semi-conductor layer 1a, and scanning-line 3a functions as a gate electrode. Thus, TFT30 for pixel switching by which opposite arrangement of the scanning-line 3a was carried out as a gate electrode is formed in the crossing part of scanning-line 3a and data-line 6a at channel field 1a', respectively.

[0075] Capacity line 3b has the main track section mostly extended in the shape of a straight line along with scanning-line 3a, and the lobe projected along with data-line 6a from the part which intersects data-line 6a.

[0076] Contact hole 8a connects with the drain field of semi-conductor layer 1a electrically, contact hole 8b connects with pixel electrode 9a electrically, and especially 1st barrier layer 80a is functioning as a buffer between the drain field of semi-conductor layer 1a, and pixel electrode 9a, respectively. Contact hole 8b is behind explained in full detail in this 1st barrier layer 80a and a contact hole 8a list.

[0077] Moreover, 1st light-shielding film 11a may be prepared in the field shown by the thick wire in drawing, respectively so that it may pass along scanning-line 3a, capacity line 3b, and the TFT30 bottom. Respectively, 1st light-shielding film 11a is good for the part which intersects data-line 6a to form in the method of drawing Nakashita broadly, to see channel field 1a' of TFT30 for pixel switching from a TFT array substrate side by this broad part, and to make it prepare in a wrap location, respectively while forming it in the shape of stripes along with scanning-line 3a.

[0078] Next, as shown in the sectional view of drawing 3 , the electro-optic device is equipped with the TFT array substrate 10 which constitutes an example of the substrate of while it is transparence, and the opposite substrate 20 which it is the transparence by which opposite arrangement is carried out at this, and also constitutes an example of the substrate of a way. The TFT array substrate 10 consists of for example, a quartz substrate, a glass substrate, and a silicon substrate, and the opposite substrate 20 consists of a glass substrate or a quartz substrate. Pixel electrode 9a is prepared in the TFT array substrate 10, and the orientation film 16 with which predetermined orientation processing of rubbing processing etc. was performed is formed in the bottom. Pixel electrode 9a consists of transparent conductive thin films, such as for example, ITO film. Moreover, the orientation film 16 consists of organic thin films, such as for example, a polyimide thin film.

[0079] On the other hand, it crosses to the opposite substrate 20 all over the, the counterelectrode 21 is formed, and the orientation film 22 with which predetermined orientation processing of rubbing processing etc. was performed is formed in the bottom. A counterelectrode 21 consists of transparent conductive thin films, such as for example, ITO film. Moreover, the orientation film 22 consists of organic thin films, such as a polyimide thin film.

[0080] TFT30 for pixel switching which carries out switching control of each pixel electrode 9a is formed in the location which adjoins each pixel electrode 9a at the TFT array substrate 10.

[0081] As further shown in the opposite substrate 20 at drawing 3 , the 2nd light-shielding film 23 is formed in the non-opening field of each pixel. For this reason, incident light does not invade into channel field 1a' of semi conductor layer 1a of TFT30 for pixel switching, low concentration source field 1b, and low concentration drain field 1c from the opposite substrate 20 side. Furthermore, the 2nd light-shielding film 23 has functions, such as color mixture prevention of the color material at the time of forming improvement in contrast, and a color filter.

[0082] Thus, it is constituted, and between the TFT array substrates 10 and the opposite substrates 20 which have been arranged so that pixel electrode 9a and a counterelectrode 21 may meet, the liquid crystal which is an example of electrooptic material is enclosed with the space surrounded by the below-mentioned sealant, and the liquid crystal layer 50 is formed. The liquid crystal layer 50 takes a predetermined orientation condition with the orientation film 16 and 22 in the condition that the electric field from pixel electrode 9a are not impressed. The liquid crystal layer 50 consists of liquid crystal which mixed the pneumatic liquid crystal of a kind or some kinds. It is the adhesives which consist of a photo-setting resin or thermosetting resin in order that a sealant may stick the TFT array substrate 10 and the opposite substrate 20 around those, and gap material, such as glass fiber for making distance between both substrates into a predetermined value or a glass bead, is mixed.

[0083] Furthermore, as shown in drawing 3 , in the location which counters TFT30 for pixel switching respectively, it is good between the TFT array substrate 10 and each TFT30 for pixel switching to prepare 1st

light-shielding film 11a. 1st light-shielding film 11a consists of a metal simple substance containing at least one of Ti, Cr, W, Ta, Mo, and Pb(s) which are a desirable opaque refractory metal, an alloy, metal silicide, etc. If constituted from such an ingredient, 1st light-shielding film 11a is destroyed by high temperature processing in the formation process of TFT30 for pixel switching performed after the formation process of 1st light-shielding film 11a on the TFT array substrate 10, or it can avoid fusing by it. Since 1st light-shielding film 11a is formed, the situation in which the reflected light (return light) from the TFT array substrate 10 side etc. carries out incidence to channel field 1a' of TFT30 for pixel switching, low concentration source field 1b, and low concentration drain field 1c can be prevented, and the property of TFT30 for pixel switching does not change with generating of the current by the light resulting from this, or it does not deteriorate.

[0084] In addition, 1st light-shielding film 11a formed in the shape of stripes may be installed for example, in the bottom of scanning-line 3a, and may be electrically connected to a constant potential line. Thus, if constituted, potential fluctuation of 1st light-shielding film 11a will not have a bad influence on 1st light-shielding film 11a to TFT30 for pixel switching by which opposite arrangement is carried out. In this case, the constant potential line supplied to constant potential lines, such as a negative supply supplied to the circumference circuits (for example, a scanning-line drive circuit, a data-line drive circuit, etc.) for driving the electro-optic device concerned as a constant potential line and a positive supply, a touch-down power source, and a counterelectrode 21 is mentioned. In addition, 1st light-shielding film 11a may be formed by the shape of a grid along with data-line 6a and scanning-line 3a, and it may be formed in the shape of an island so that channel field 1a' of TFT30 for pixel switching, low concentration source field 1b, and low concentration drain field 1c may be covered at least.

[0085] Furthermore, the substrate insulator layer 12 is formed between 1st light-shielding film 11a and two or more TFT30 for pixel switching. The substrate insulator layer 12 is formed in order to insulate electrically semi conductor layer 1a which constitutes TFT30 for pixel switching from 1st light-shielding film 11a. Furthermore, the substrate insulator layer 12 also has a function as substrate film for TFT30 for pixel switching by being formed all over the TFT array substrate 10. That is, it has the function to prevent degradation of the property of TFT30 for pixel switching with the dry area at the time of polish of the front face of the TFT array substrate 10, the dirt which remains after washing. The substrate insulator layer 12 consists of high insulation glass, such as NSG (non doped silicate glass), PSG (phosphorus silicate glass), BSG (boron silicate glass), and BPSG (boron phosphorus silicate glass), or silicon oxide film, a silicon nitride film, etc. The substrate insulator layer 12 can also protect the situation where 1st light-shielding film 11a pollutes the TFT30 grade for pixel switching.

[0086] 1st storage capacitance 70a is constituted by considering as the 1st dielectric film which considered as the 1f of the 1st storage capacitance electrodes, used as the 2nd storage capacitance electrode a part of capacity line 3b which counters this, installed [semi-conductor layer 1a was installed from high concentration drain field 1e, and] the insulating thin film 2 containing gate dielectric film with this operation gestalt from the location which counters scanning-line 3a, and was pinched by inter-electrode [these]. Furthermore, a part of this 2nd storage capacitance electrode and 1st barrier layer 80a which counters are used as the 3rd storage capacitance electrode, and the 1st interlayer insulation film 81 is formed in inter-electrode [these]. The 1st interlayer insulation film 81 functions as the 2nd dielectric film, and 2nd storage capacitance 70b is formed. And parallel connection of these 1st storage capacitance 70a and the 2nd are recording **** 70b is carried out through contact hole 8a, and storage capacitance 70 is constituted. Since especially the insulating thin film 2 as the 1st dielectric film of 1st storage capacitance 70a is exactly gate dielectric film of TFT30 formed on the polish recon film of high temperature oxidation, it can be made into the thin insulator layer of high pressure-proofing, and can constitute 1st storage capacitance 70a from small area as mass storage capacitance comparatively. Moreover, since the 1st interlayer insulation film 81 can also be formed more thinly than the insulating thin film 2 as well as [or] the insulating thin film 2, 2nd storage capacitance 70b can constitute it as storage capacitance mass in small area comparatively. Therefore, let storage capacitance 70 which consists of these 1st storage capacitance 70a and 2nd storage capacitance 70b in three dimensions be storage capacitance mass in small area, using effectively the tooth space which separated from a pixel opening field called the field (namely, field in which capacity line 3b was formed) which the disclination of liquid crystal generates along with the field under data-line 6a, and scanning-line 3a.

[0087] Thus, the silicon oxide film, a silicon nitride film, etc. are sufficient as the 1st interlayer insulation film 81 which constitutes 2nd storage capacitance 70b, and it may consist of multilayers. The 1st interlayer

insulation film 81 can be formed with various kinds of well-known techniques (a reduced pressure CVD method, a plasma-CVD method, the oxidizing [thermally] method, etc.) used for generally forming the insulating thin films 2, such as gate dielectric film. Since the path of contact hole 8a can be made still smaller by forming the 1st interlayer insulation film 81 thinly, the hollow and irregularity of 1st barrier layer 80a in contact hole 8a mentioned above are still smaller, it ends, and flattening in pixel electrode 9a located in the upper part is promoted further.

[0088] In drawing 3 TFT30 for pixel switching It has LDD (Lightly Doped Drain) structure. Channel field 1a' of semi-conductor layer 1a in which a channel is formed of the electric field from scanning-line 3a and concerned scanning-line 3a, 1d list of high concentration source fields of low concentration source field 1b of the insulating thin film 2 containing the gate dielectric film with which scanning-line 3a and semi-conductor layer 1a are insulated, data-line 6a, and semi-conductor layer 1a and low concentration drain field 1c, and semi-conductor layer 1a is equipped with high concentration drain field 1e. One to which it corresponds of two or more pixel electrode 9a relays 1st barrier layer 80a to high concentration drain field 1e, and it is electrically connected to it. Low concentration drain field 1c and high concentration drain field 1e are formed in low concentration source field 1b and 1d list of high concentration source fields to semi-conductor layer 1a like the after-mentioned by doping the impurity the object for n molds of predetermined concentration, or for p molds according to whether the channel of n mold or p mold is formed. TFT of an n-type channel has the advantage that a working speed is quick, and it is used as TFT30 for pixel switching which is the switching element of a pixel in many cases. this operation gestalt -- especially -- data-line 6a -- aluminum etc. -- low -- it consists of protection-from-light nature and conductive thin films, such as metal membrane metallurgy group silicide [****]. [, such as alloy film,] Moreover, on 1st barrier layer 80a and the 1st interlayer insulation film 81, the 2nd interlayer insulation film 4 with which contact hole 8b which leads to the contact hole 5 and 1st barrier layer 80a which lead to 1d of high concentration source fields was formed respectively is formed. Data-line 6a is electrically connected to 1d of high concentration source fields through the 1d [of this high concentration source field] contact hole 5. Furthermore, on data-line 6a and the 2nd interlayer insulation film 4, the 3rd interlayer insulation film 7 with which contact hole 8b to 1st barrier layer 80a was formed is formed. Through this contact hole 8b, it connects with 1st barrier layer 80a electrically, and pixel electrode 9a relays 1st barrier layer 80a further, and is electrically connected to high concentration drain field 1e through contact hole 8a. The above-mentioned pixel electrode 9a is prepared in the top face of the 3rd interlayer insulation film 7 constituted in this way.

[0089] Although TFT30 for pixel switching has LDD structure as mentioned above preferably, it may be TFT of the self aryne mold which may have the offset structure which does not drive an impurity into low concentration source field 1b and low concentration drain field 1c, drives in an impurity by high concentration by using as a mask the gate electrode which consists of a part of scanning-line 3a, and forms the high concentration source and a drain field in self align.

[0090] Moreover, although considered as the single gate structure which has arranged one gate electrode of TFT30 for pixel switching among 1d [of high concentration source fields], and high concentration drain field 1e with this operation gestalt, two or more gate electrodes may be arranged among these. Under the present circumstances, to each gate electrode, the same signal is made to be impressed. Thus, if TFT is constituted above the dual gate or the triple gate, the leakage current of a joint with a channel, the source, and a drain field can be prevented, and the current at the time of OFF can be reduced. If at least one of these gate electrodes is made into LDD structure or offset structure, the OFF state current can be reduced further and the stable switching element can be obtained.

[0091] As shown in drawing 2 and drawing 3 , since high concentration drain field 1e and pixel electrode 9a are electrically connected via 1st barrier layer 80a through contact hole 8a and contact hole 8b, in the electro-optic device of this operation gestalt, the path of contact hole 8a and contact hole 8b can be made small from pixel electrode 9a to a drain field as compared with the case where one contact hole is punctured, respectively. That is, etching precision must stop the dry etching which can make the path of a contact hole small on the way, and when puncturing one contact hole, in order to fall (for example, in order to prevent the thrust omission in about 50nm very thin semi-conductor layer 1a), it must construct a process so that it may finally puncture to semi-conductor layer 1a by wet etching, so that a contact hole is punctured deeply. Or it will be necessary to be based on dry etching, to run and to prepare the polish recon film for prevention separately.

[0092] On the other hand, with this operation gestalt, since what is necessary is just to connect pixel electrode 9a and high concentration drain field 1e by two in-series contact hole 8a and contact hole 8b, it becomes possible to puncture these contact hole 8a and contact hole 8b by dry etching, respectively. Or it becomes possible to shorten distance punctured by wet etching at least. However, in order to attach some taper to contact hole 8a and contact hole 8b, it may dare to be made to perform short-time wet etching after dry etching comparatively.
[0093] Since the hollow and irregularity which the path of contact hole 8a and contact hole 8b can be made small, respectively, and are formed in the front face of 1st barrier layer 80a in contact hole 8a are also small and end according to this operation gestalt as mentioned above, flattening in the part of pixel electrode 9a located in the upper part is promoted to some extent. Furthermore, since the hollow and irregularity which are formed in the front face of pixel electrode 9a in 2nd contact hole 8b are also small and end, flattening in the part of this pixel electrode 9a is promoted to some extent.
[0094] 1st barrier layer 80a consists of a conductive light-shielding film especially with this operation gestalt. Therefore, 1st barrier layer 80a enables it to specify each pixel opening field partially at least. For example, 1st barrier layer 80a consists of a metal simple substance containing at least one of Ti, Cr, W, Ta, Mo, and Pb(s) which are an opaque refractory metal, an alloy, metal silicide, etc. Thereby, connection electric good can be taken through contact hole 8b between 1st barrier layer 80a and pixel electrode 9a. As for the thickness of 1st barrier layer 80a, it is desirable to consider for example, as 50nm or more 500nm or less extent. or [that the irregularity of the front face of pixel electrode 9a which possibility of running at the time of puncturing of 2nd contact hole 8b in a manufacture process if there is thickness of about 50nm became low, and originated in existence of 1st barrier layer 80a when it was about 500nm does not serve as a between title] -- or it is because flattening is comparatively easily possible.
[0095] With this operation gestalt, furthermore, the right-and-left side of the field which met data-line 6a among the pixel Sekiguchi fields in each pixel It has specified from the data-line 6a part in island-like 2nd barrier layer 80b and the contact hole 5 circumference which are extended in the shape of straight side along with data-line 6a. 1st barrier layer 80a and 1st light-shielding film 11a have prescribed the surface and the lower side of a field which met scanning-line 3a and capacity line 3b among the pixel opening fields in each pixel, respectively.
[0096] As more specifically shown in drawing 2 and drawing 4 , 2nd barrier layer 80b is seen superficially, is partially arranged in the gap of pixel electrode 9a, and, also partially, has lapped with pixel electrode 9a. For this reason, by piling up a part of this pixel electrode 9a and 2nd barrier layer 80b can prescribe the great portion of right-and-left side of the pixel opening field in each pixel. Under the present circumstances, especially in the part where the pixel opening field was specified by 2nd barrier layer 80b, since it sees superficially and there is no clearance between pixel electrode 9a and 2nd barrier layer 80b, the optical leakage through such a clearance does not take place. Consequently, finally a contrast ratio is raised. Since data-line 6a does not need to prescribe a pixel opening field in the part where the pixel opening field was specified to coincidence by 2nd barrier layer 80b, in this part, the width of face of data-line 6a has been narrowed a little rather than the width of face of 2nd barrier layer 80b. Consequently, as shown in drawing 4 , when making it data-line 6a and pixel electrode 9a not lap through the 3rd interlayer insulation film 7, it is not necessary to generate the parasitic capacitance between the sources of TFT30 and the drains in each pixel. For this reason, it originates in the potential shake concerned of data-line 6a which sways frequently to the potential of the picture signal supplied in predetermined periods, such as one etc. frame, TFT30 of an other bank, TFT30 carries out abnormality actuation with the parasitic capacitance between the above-mentioned source and a drain, and the situation which the electrical potential difference which should be made to hold to pixel electrode 9a leaks can be prevented. The flicker and line nonuniformity in a display image can be reduced these results. however -- the comparatively small field of the contact hole 5 circumference where 2nd barrier layer 80b does not exist -- the width of face of data-line 6a -- some -- thicker ** -- it may be made like and data-line 6a may prescribe a pixel opening field.
[0097] Moreover, if it constitutes so that a pixel opening field may be specified as mentioned above, since it is not necessary to form the 2nd light-shielding film 23 in the opposite substrate 20, it is possible to reduce the cost of an opposite substrate. Furthermore, the fall and dispersion of a pixel numerical aperture by the alignment gap with the opposite substrate 20 and the TFT array substrate 10 can be prevented. Moreover, when forming the 2nd light-shielding film 23 in the opposite substrate 20 Even if it forms more smallish so that a pixel

numerical aperture may not be reduced by the alignment gap with the TFT array substrate 10, as mentioned above Data-line 6a, In order for the film of the protection-from-light nature formed in 1st barrier layer 80a and a 2nd barrier layer 80b list at the TFT array substrate [1st light-shielding film 11a] 10 side to prescribe the pixel Sekiguchi section, Pixel opening can be specified with a sufficient precision and a pixel numerical aperture can be raised compared with the case where pixel opening is decided from 2nd light-shielding film 23 ** on the opposite substrate 20.

[0098] Furthermore, by considering as the configuration which narrows the width of face of data-line 6a a little, and does not lap with a part for the edge of pixel electrode 9a as shown in drawing 2 and drawing 4 Generating of defects, such as electric short-circuit between both with high possibility of generating in the part with which data-line 6a and pixel electrode 9a lapped through the 3rd interlayer insulation film 7 (short circuit), can be suppressed, and, finally decline in the rate of an equipment defect and the improvement in the yield at the time of manufacture are slippery.

[0099] 2nd barrier layer 80b is preferably connected to capacity line 3b or other constant potential lines electrically. That is, since the amount of [of a part for a edge and pixel electrode 9a of 2nd barrier layer 80b] edge laps, some parasitic capacitance is added among both, but if the potential of 2nd barrier layer 80b is maintained at fixed potential, the bad influence which potential fluctuation of 2nd barrier layer 80b has on the potential of pixel electrode 9a can be reduced. In addition, with this operation gestalt, contact hole 8c for connecting electrically 2nd barrier layer 80b and capacity line 3b can be punctured according to the same process as the process which punctures contact hole 8a, and does not cause complication of a manufacture process. In addition, 2nd barrier layer 80b is electrically connected to capacity line 3b through contact hole 8c in this case for every pixel.

[0100] Furthermore, in the configuration by which opposite arrangement of 2nd barrier layer 80b and the data-line 6a was carried out through the 2nd interlayer insulation film 4 again like ****, capacity is added to data-line 6a between 2nd barrier layer 80b by which potential was stabilized more. For this reason, the capacity of data-line 6a can be set as moderate magnitude which does not cause a potential shake. Even if it makes especially a pixel pitch detailed and makes detailed width of face of data-line 6a in connection with this, the lack of capacity of data-line 6a can be suppressed by making the capacity between 2nd barrier layer 80b increase. Thereby, the write-in deficiency in performance in supply to pixel electrode 9a of the picture signal through data-line 6a can be prevented. In other words, the structure where data-line 6a advantageous in case especially a pixel pitch is made detailed becomes strong to a noise is acquired comparatively easily.

[0101] In addition, although the other shape of a round shape, a square, or a polygon etc. has as the flat-surface configuration of each contact hole (8a, 8b, 8c, and 5) of this operation gestalt, especially a round shape is useful to the crack prevention in the interlayer insulation film around a contact hole etc. And in order to obtain connection electric good, it is desirable to perform wet etching after dry etching and to attach some taper to these contact holes, respectively.

[0102] As explained above, while giving the function to relay TFT30 and pixel electrode 9a to 1st barrier layer 80a according to the electro-optic device of the 1st operation gestalt Since the function to specify a pixel opening field is given closing adequate supply of a picture signal to it if to 2nd barrier layer 80b which consists of the same film as this 1st barrier layer 80a, low cost-ization can be attained in the simplification list of a laminated structure and a manufacture process as a whole.

[0103] (Manufacture process of the electro-optic device in the 1st operation gestalt) Next, the manufacture process of the TFT array substrate which constitutes the electro-optic device in an operation gestalt with the above configurations is explained with reference to drawing 8 from drawing 5 . In addition, it is process drawing which drawing 8 makes each class by the side of the TFT array substrate in each process correspond to the A-A' cross section of drawing 2 like drawing 3 from drawing 5 , and is shown.

[0104] As first shown in the process (1) of drawing 5 , the TFT array substrates 10, such as a quartz substrate, a hard glass substrate, and a silicon substrate, are prepared. Here, it heat-treats preferably at inert gas ambient atmospheres, such as N2 (nitrogen), and an about 900-1300-degree C elevated temperature, and it pretreats so that distortion produced in the TFT array substrate 10 in the elevated-temperature process carried out behind may decrease. That is, according to the temperature by which high temperature processing is carried out at the maximum elevated temperature in a manufacture process, the TFT array substrate 10 is heat-treated at the same temperature or the temperature beyond it in advance. and the whole surface of the TFT array substrate 10

processed in this way -- metal alloy film, such as metal metallurgy group silicide, such as Ti, Cr, W, Ta, Mo, and Pb, -- sputtering etc. -- about 100-500nm thickness -- the light-shielding film 11 of about 200nm thickness is formed preferably. In addition, on a light-shielding film 11, in order to ease surface reflection, antireflection films, such as polish recon film, may be formed.

[0105] Next, as shown in a process (2), 1st light-shielding film 11a is formed by forming the resist mask corresponding to the pattern of 1st light-shielding film 11a by the photolithography on the this formed light-shielding film 11, and etching to a light-shielding film 11 through this resist mask.

[0106] As shown in a process (3), with ordinary pressure or a reduced pressure CVD method on 1st light-shielding film 11a Next, TEOS (tetrapod ethyl orthochromatic silicate) gas, TEB (tetrapod ethyl boat rate) gas, TMOP (tetrapod methyl oxy-FUOSU rate) gas, etc. are used. The substrate insulator layer 12 which consists of silicate glass film, such as NSG (non silicate glass), PSG (phosphorus silicate glass), BSG (boron silicate glass), and BPSG (PORON phosphorus silicate glass), a silicon nitride film, silicon oxide film, etc. is formed. The thickness of this substrate insulator layer 12 may be about 500-2000nm.

[0107] Next, as shown in a process (4), about 450-550 degrees C of amorphous silicon film are preferably formed comparatively on the substrate insulator layer 12 with the reduced pressure CVD (for example, CVD with a pressure of about 20-40Pa) using the mono-silane gas of flow rate about 400 to 600 cc/min, disilane gas, etc. of about 500 degrees C in a low-temperature environment. Then, in nitrogen-gas-atmosphere mind, by performing heat treatment of 4 - 6 hours preferably at about 600-700 degrees C for about 1 to 10 hours, solid phase growth of the polish recon film 1 is carried out until it becomes the thickness of about 100nm preferably in about 50-200nm thickness. As an approach of carrying out solid phase growth, heat treatment using RTA (Rapid Thermal Anneal) is sufficient, and laser heat treatment using an excimer laser etc. is sufficient.

[0108] Under the present circumstances, as TFT30 for pixel switching shown in drawing 3 , when creating TFT30 for pixel switching of an n channel mold, the impurity of V group elements, such as Sb (antimony), As (arsenic), and P (Lynn), may be slightly doped by an ion implantation etc. to the channel field concerned. Moreover, when using TFT30 for pixel switching as a p channel mold, the impurity of III group elements, such as B (boron), Ga (gallium), and In (indium), may be slightly doped by an ion implantation etc. In addition, the polish recon film 1 may be directly formed with a reduced pressure CVD method etc. without passing through the amorphous silicon film. Or drive silicon ion into the polish recon film deposited with the reduced pressure CVD method etc., once make it amorphous, it is made to recrystallize by the postheat treatment etc., and the polish recon film 1 may be formed.

[0109] Next, as shown in a process (5), semi-conductor layer 1a which has a predetermined pattern containing the 1f of the 1st storage capacitance electrodes according to a photolithography process, an etching process, etc. is formed.

[0110] As shown in a process (6), semi-conductor layer 1a which constitutes TFT30 for pixel switching next, the temperature of about 900-1300 degrees C, and by oxidizing thermally with the temperature of about 1000 degrees C preferably As thermal oxidation silicon film 2a with a comparatively thin thickness of about 30nm is formed and it is further shown in a process (7) Insulator layer 2b which consists of high-temperature-oxidation silicon film (HTO film) or a silicon nitride film with a reduced pressure CVD method etc. is deposited on the comparatively thin thickness of about 50nm. The insulating thin film 2 which contains the 1st dielectric film for storage capacitance formation with the gate dielectric film with the multilayer structure containing thermal oxidation silicon film 2a and insulator layer 2b of TFT30 for pixel switching is formed. consequently, the thickness of semi-conductor layer 1a -- the thickness of about 30-150nm -- desirable -- the thickness of about 35-50nm -- becoming -- the thickness of the insulating thin film 2 -- the thickness of about 20-150nm -- it becomes the thickness of about 30-100nm preferably. Thus, by shortening elevated-temperature thermal oxidation time amount, when using especially an about 8 inches large-sized substrate, the camber by heat can be prevented. However, the insulating thin film 2 with monolayer structure may be formed only by oxidizing the polish recon film 1 thermally.

[0111] Next, as shown in a process (8), after forming the resist layer 500 according to a photolithography process, an etching process, etc. on semi-conductor layer 1a except the part used as the 1f of the 1st storage capacitance electrodes, P ion is doped in about 3x1012/cm2 of doses, and the 1f of the 1st storage capacitance electrodes is formed into low resistance.

[0112] Next, as shown in a process (9), after removing the resist layer 500, the polish recon film 3 is deposited

with a reduced pressure CVD method etc., thermal diffusion of the P is carried out further, and the polish recon film 3 is electric-conduction-ized. or the polish recon film 3 formed simultaneously introduced P ion -- low -- the polish recon film [****] may be used. The thickness of the polish recon film 3 is preferably deposited on about 300nm in about 100-500nm thickness.

[0113] Next, as shown in the process (10) of drawing 6 , capacity line 3b is formed with scanning-line 3a of a predetermined pattern according to a photolithography process, an etching process, etc. using a resist mask. Scanning-line 3a and capacity line 3b are good also as a multilayer interconnection which could form by metal alloy film, such as refractory metal metallurgy group silicide, and was combined with the polish recon film etc.

[0114] Next, as shown in a process (11), when TFT30 for pixel switching shown in drawing 3 is set to TFT of an n channel mold with LDD structure, In order to form low concentration source field 1b and low concentration drain field 1c in semi-conductor layer 1a first, by using as a mask the gate electrode which consists of a part of scanning-line 3a, it is low concentration about the impurity of V group elements, such as P, for example, P ion is doped with the dose of one to 3x1013-/cm2. Thereby, semi-conductor layer 1a under scanning-line 3a becomes channel field 1a'. Capacity line 3b and scanning-line 3a are also formed into low resistance by the dope of this impurity.

[0115] Next, as shown in a process (12), in order to form 1d of high concentration source fields and high concentration drain field 1e which constitute TFT30 for pixel switching, after forming the resist layer 600 on scanning line 3a with a mask with wide width of face rather than scanning line 3a, similarly it be high concentration about the impurity of V group elements, such as P, for example, P ion be doped with the dose of 1 - 3x1015-/cm2. Moreover, to semi-conductor layer 1a, when using TFT30 for pixel switching as a p channel mold, in order to form 1d of high concentration source fields, and high concentration drain field 1e in low concentration source field 1b and a low concentration drain field 1c list, the impurity of III group elements, such as B, is used and doped. In addition, it is good also as TFT of offset structure, without, for example, performing a low-concentration dope, and it is good also as TFT of a self aryne mold by the ion-implantation technique using P ion, B ion, etc., using scanning-line 3a as a mask. Capacity line 3b and scanning-line 3a are also further formed into low resistance by the dope of this impurity.

[0116] In addition, in parallel to these component formation processes of TFT30, circumference circuits with the **** type structure which consists of an n channel mold TFT and a p channel mold TFT, such as a data-line drive circuit and a scanning-line drive circuit, may be formed in the periphery on the TFT array substrate 10. Thus, if semi-conductor layer 1a which constitutes TFT30 for pixel switching in this operation gestalt is formed by the polish recon film, at the time of formation of TFT30 for pixel switching, it is the same process mostly, and a circumference circuit can be formed and it is advantageous on manufacture.

[0117] Next, as shown in a process (13), after removing the resist layer 600, the 1st interlayer insulation film 81 which consists of high-temperature-oxidation silicon film (HTO film) or a silicon nitride film by the reduced pressure CVD method, a plasma-CVD method, etc. is deposited [capacity line 3b and a scanning-line 3a list] on the insulating thin film 2 at the comparatively thin thickness of about 200nm or less. However, as mentioned above, the 1st interlayer insulation film 81 may be constituted from multilayers, and can form the 1st interlayer insulation film 81 with various kinds of well-known techniques used for generally forming the gate dielectric film of TFT.

[0118] Next, as shown in a process (14), contact hole 8c for connecting electrically 2nd barrier layer 80b and capacity line 3b to the contact hole 8a list for connecting electrically 1st barrier layer 80a and high concentration drain field 1e is formed by dry etching, such as reactive ion etching and reactant ion beam etching. Since such dry etching has high directivity, it can puncture contact hole 8a and contact hole 8c of a small path. Or wet etching advantageous to preventing that contact hole 8a runs through semi-conductor layer 1a may be used together. This wet etching is effective also from a viewpoint which gives the taper for taking connection more electric to fitness to contact hole 8a. Moreover, especially contact hole 8a and contact hole 8c can be punctured to coincidence like, and are advantageous to **** on manufacture.

[0119] Next, as shown in a process (15), all over capacity line 3b looked into through high concentration drain field 1e and contact hole 8c which are looked into through contact hole 8a in 1st interlayer insulation film 81 list, metal alloy film, such as metal metallurgy group silicide, such as Ti, Cr, W, Ta, Mo, and Pb, is deposited by sputtering etc., and the electric conduction film 80 of about 50-500nm thickness is formed. If there is thickness of about 50nm, there will almost be no possibility of running when puncturing contact hole 8b behind.

In addition, on this electric conduction film 80, in order to ease surface reflection, antireflection films, such as polish recon film, may be formed. In addition, the electric conduction film 80 may be the multilayers which carried out the laminating of the metal alloy film or polish recon film, such as metal metallurgy group silicide.
[0120] Next, as shown in the process (16) of drawing 7 , 1st barrier layer 80a and 2nd barrier layer 80b are formed by performing a photolithography process, an etching process, etc. on the this formed electric conduction film 80. As especially 2nd barrier layer 80b was shown in drawing 4 here, it is good to form so that it may lap pixel electrode 9a in which the part is formed later, and a little.
[0121] Next, as shown in a process (17), the 2nd interlayer insulation film 4 which consists of silicate glass film, such as NSG, PSG, BSG, and BPSG, a silicon nitride film, silicon oxide film, etc. is formed using ordinary pressure or a reduced pressure CVD method, TEOS gas, etc. so that 1st barrier layer 80a and 2nd barrier layer 80b may be covered in 1st interlayer insulation film 81 list. The thickness of the 2nd interlayer insulation film 4 has desirable about 500-1500nm. If there is 500nm or more of thickness of the 2nd interlayer insulation film 4, the parasitic capacitance between data-line 6a and scanning-line 3a will remain, or will hardly pose a problem.
[0122] Next, in order to activate semi-conductor layer 1a, after heat-treating about 10000-degreeC about 20 minutes in the phase of a process (18), the contact hole 5 for connecting electrically high concentration drain field 1e of data-line 6a and semi-conductor layer 1a is punctured to the insulating thin film 2, the 1st interlayer insulation film 81, and the 2nd interlayer insulation film 4. Moreover, the contact hole for connecting with wiring which illustrates neither scanning-line 3a nor capacity line 3b in a substrate boundary region can also be punctured according to the same process as a contact hole 5.
[0123] Next, as shown in a process (19), it deposits preferably in about 100-500nm thickness by sputtering etc. on the 2nd interlayer insulation film 4 at about 300nm by making low resistance metal metallurgy group silicide, such as aluminum of protection-from-light nature, etc. into a metal membrane 6.
[0124] Next, as shown in a process (20), data-line 6a is formed according to a photolithography process, an etching process, etc. As especially data-line 6a was shown in drawing 4 R> 4 here, it forms so that it may not lap with pixel electrode 9a formed later, and so that it may lap with 2nd barrier layer 80b.
[0125] Next, as shown in the process (21) of drawing 8 , the 3rd interlayer insulation film 7 which consists of silicate glass film, such as NSG, PSG, BSG, and BPSG, a silicon nitride film, silicon oxide film, etc. is formed using ordinary pressure or a reduced pressure CVD method, TEOS gas, etc. so that a data-line 6a top may be covered. The thickness of the 3rd interlayer insulation film 7 has desirable about 500-1500nm.
[0126] Next, as shown in a process (22), contact hole 8b for connecting electrically pixel electrode 9a and 1st barrier layer 80a is formed by dry etching, such as reactive ion etching and reactant ion beam etching. Wet etching may be added in order to make it the shape of a taper.
[0127] Next, on the 3rd interlayer insulation film 7, as shown in a process (23), as the transparent conductive thin films 9, such as ITO film, are deposited on the thickness of about 50-200nm and are further shown in a process (24) by sputtering etc., pixel electrode 9a is formed according to a photolithography process, an etching process, etc. In addition, when using the electro-optic device concerned as a reflective mold, pixel electrode 9a may be formed from an opaque ingredient with high reflection factors, such as aluminum.
[0128] As explained above, according to the manufacture process in this operation gestalt, the electro-optic device of the 1st operation gestalt which is a comparatively small routing counter and was mentioned above using each comparatively easy process can be manufactured.
[0129] (The 2nd operation gestalt) The configuration of the electro-optic device in the 2nd operation gestalt of this invention is explained with reference to drawing 11 from drawing 9 . Drawing 9 is a top view of two or more pixel groups where the TFT array substrate with which the data line in the 2nd operation gestalt, the scanning line, a pixel electrode, etc. were formed adjoins each other, drawing 10 is the A-A' sectional view, and drawing 11 is the B-B' sectional view. Moreover, in order to make each class and each part material into the magnitude of extent which can be recognized on a drawing, scales are made to have differed for each class or every each part material in drawing 10 and drawing 11 . In addition, about the same component as the 1st operation gestalt shown in drawing 4 from drawing 2 in the 2nd operation gestalt shown in drawing 11 from drawing 9 , the same reference mark is attached and the explanation is omitted.
[0130] It has junction conductive layer 6b which is electrically connected to high concentration drain field 1e of semi-conductor layer 1a through contact hole 88a with the 2nd operation gestalt in drawing 11 from drawing 9 ,

and consisted of same layers as data-line 6a, and 1st barrier layer 90a which consists of a conductive layer of the protection-from-light nature electrically connected to pixel electrode 9a through contact hole 88c. And opposite arrangement is carried out through the 2nd interlayer insulation film 4 formed on data-line 6a and junction conductive layer 6b, and junction conductive layer 6b and 1st barrier layer 90a are mutually connected electrically through contact hole 88b punctured by this 2nd interlayer insulation film 4. On the other hand, with the 2nd operation gestalt, 2nd barrier layer 90b which consists of a conductive layer of the same protection-from-light nature as 1st barrier layer 90a is prepared, and 2nd barrier layer 90b and capacity line 3b are electrically connected through contact hole 88d. It can substitute as a capacity line by using 2nd barrier layer 90b as a storage capacitance electrode, and connecting it with an adjoining pixel group by this. In this case, you may form in the shape of an island for every pixel by using capacity line 3b as a storage capacitance electrode. Thereby, a pixel numerical aperture can be enlarged. Moreover, by connecting electrically 2nd barrier layer 90b and capacity line 3b, it can be double, a capacity line can be formed and redundant structure can be realized. As shown in drawing 9 , except for the perimeter of the field where it sees superficially and 1st barrier layer 90a exists, the gap of pixel electrode 9a is established in 2nd barrier layer 90b in the shape of a wrap grid, and it specifies the right-and-left side and the vertical side which met data-line 6a and scanning-line 3a among pixel opening fields, respectively. Also in this case, a part for the edge of 2nd barrier layer 90b is put on a part for the edge of pixel electrode 9a a little as well as the case of the 1st operation gestalt. In addition, about the gap of 1st barrier layer 90a and 2nd barrier layer 90b, optical leakage can be easily prevented by covering by the 2nd light-shielding film 23 by the side of junction conductive layer 6b or an opposite substrate. About other configurations, it is the same as that of the case of the 1st operation gestalt.

[0131] Thus, with the 2nd operation gestalt, junction becomes possible good about from pixel electrode 9a to semi-conductor layer 1a by junction conductive layer 6b and 1st barrier layer 90a which are two conductive layers for junction. When pixel electrode 9a consists of ITO film and data-line 6a consists of aluminum film especially, it is desirable to constitute from refractory metals, such as Ti, Cr, W, etc. from which connection electric good is obtained among both, etc.

[0132] Moreover, as shown in drawing 11 , in the configuration by which data-line 6a was pinched through the 1st interlayer insulation film 81 and the 2nd interlayer insulation film 4 which are a dielectric film between capacity line 3b and barrier layer 90b, capacity is added to data-line 6a between capacity line 3b and 2nd barrier layer 90b by which potential was stabilized more. For this reason, the capacity of data-line 6a can be set as moderate magnitude which does not cause a potential shake, and the write-in deficiency in performance in supply to pixel electrode 9a of the picture signal through data-line 6a can be prevented.

[0133] Junction conductive layer 6b which consists of the same film as such aluminum film For example, it sets at the process (18) in the manufacture process of the 1st operation gestalt. Puncture contact hole 88a which results in high concentration drain field 1e, and in a process (20), although junction conductive layer 6b is formed above high concentration drain field 1e including the part of this contact hole 88a What is necessary is just to give a photolithography process, an etching process, etc. to aluminum film formed at the process (19). What is necessary is just to form according to the same process as a process (16) from the process (13) in the 1st operation gestalt furthermore at 2nd interlayer insulation film 4 list on data-line 6a and junction conductive layer 6b about 1st barrier layer 90a and 2nd barrier layer 90b.

[0134] (The 3rd operation gestalt) The configuration of the electro-optic device in the 3rd operation gestalt of this invention is explained with reference to drawing 12 . Drawing 12 is a sectional view corresponding to the sectional view in which the data line in the 3rd operation gestalt, the scanning line, a pixel electrode, etc. were formed. Moreover, in order to make each class and each part material into the magnitude of extent which can be recognized on a drawing, scales are made to have differed for each class or every each part material in drawing 12 . In addition, about the same component as the 2nd operation gestalt shown in drawing 10 in the 3rd operation gestalt shown in drawing 12 , the same reference mark is attached and the explanation is omitted.

[0135] In drawing 12 , without using junction conductive layer 6b unlike the 2nd operation gestalt, it consists of 3rd operation gestalten so that electric connection can be taken between direct high concentration drain field 1e by 1st barrier layer 90a'. About other configurations, it is the same as that of the case of the 2nd operation gestalt.

[0136] Therefore, according to the 3rd operation gestalt, trunk connection of pixel electrode 9a and the high concentration drain field 1e can be electrically carried out to the ITO film which constitutes pixel electrode 9a

by 1st barrier layer 90a' which consists of congenial refractory metal film electrically.
[0137] (The 4th operation gestalt) The configuration of the electro-optic device in the 4th operation gestalt of this invention is explained with reference to drawing 15 from drawing 13 . Drawing 13 is a top view of two or more pixel groups where the TFT array substrate with which the data line in the 4th operation gestalt, the scanning line, a pixel electrode, etc. were formed adjoins each other, drawing 14 R> 4 is the A-A' sectional view, and drawing 15 is the B-B' sectional view. Moreover, in order to make each class and each part material into the magnitude of extent which can be recognized on a drawing, scales are made to have differed for each class or every each part material in drawing 14 and drawing 15 . In addition, about the same component as the 1st operation gestalt shown in drawing 4 from drawing 2 R> 2 in the 4th operation gestalt shown in drawing 15 from drawing 13 , the same reference mark is attached and the explanation is omitted.
[0138] In drawing 15 , the gap of pixel electrode 9a where 1st light-shielding film 11a' adjoins each other unlike the 1st operation gestalt is sewn with the 4th operation gestalt from drawing 13 , it is formed in the shape of a grid, and capacity line 3b is electrically connected to 1st protection-from-light gland 11a' for every pixel through the contact hole 15. The potential of storage capacitance 70 can be stabilized by it being possible to operate 1st light-shielding film 11a' as redundancy wiring of capacity line 3b, and attaining low resistance-ization of capacity line 3b. Moreover, this configuration may constitute capacity line 3b from substituting for 1st light-shielding film 11a' as a capacity line as an island-like storage capacitance electrode for every pixel. Thereby, a pixel numerical aperture can be enlarged. Moreover, the capacity line for forming storage capacitance may be made 3-fold wiring by combining with the 2nd operation gestalt by connecting capacity line 3b with 1st light-shielding film 11a' and 2nd barrier layer 90b electrically. When forming for every pixel in the shape of an island by using capacity line 3b as a storage capacitance electrode, 1st light-shielding film 11a' and 2nd barrier layer 90b are connected with the pixel which is electrically connected through a storage capacitance electrode, and adjoins. In addition, the faulty connection in a contact hole 15 and contact hole 8c can be prevented by puncturing in the flat-surface location where contact hole 8c for connecting a contact hole 15, 2nd barrier layer 80b, and capacity line 3b differs.
[0139] Furthermore, as shown in drawing 14 and drawing 15 , wiring and a part of TFTat least 30 become depressed in a concave, TFT array substrate 10' is formed, and the top front face is formed evenly. Consequently, flattening of the front face of the 3rd interlayer insulation film 7 in the plane region in which wiring of data-line 6a, scanning-line 3a, capacity line 3b, etc. and TFT30 were formed is carried out. About other configurations, it is the same as that of the case of the 1st operation gestalt.
[0140] Therefore, according to the 4th operation gestalt, a level difference with a pixel opening field with the field where scanning-line 3a, TFT30, capacity line 3b, etc. are formed in the data line 6 in piles is reduced. Thus, since flattening of the pixel electrode 9a is carried out, the disclination of the liquid crystal layer 50 can be reduced according to the degree of the flattening concerned. Consequently, more nearly high-definition image display becomes possible and it also becomes possible to extend a pixel opening field.
[0141] In addition, it may carry out by for example, not flattening by forming a slot in such TFT array substrate 10' but CMP (Chemical Mechanincal Polishing) processing, spin coat processing, the reflow method, etc., or flattening in the 2nd interlayer insulation film 4 or the 3rd interlayer insulation film 7 may be performed using the organic SOG (Spin On Glass) film, the inorganic SOG film, the polyimide film, etc. In addition, an above-mentioned configuration is applicable also to the 1st operation gestalt, the 2nd operation gestalt, and the 3rd operation gestalt.
[0142] (The whole electro-optic device configuration) The whole electro-optic device configuration in each operation gestalt constituted as mentioned above is explained with reference to drawing 16 and drawing 17 . In addition, drawing 16 is the top view which looked at the TFT array substrate 10 from the opposite substrate 20 side with each component formed on it, and drawing 1717 is a H-H' sectional view of drawing 16 .
[0143] In drawing 16 , on the TFT array substrate 10, the sealant 52 is formed along the edge and the 3rd light-shielding film 53 as a frame which specifies the circumference of the image display field which consists of an ingredient which is the same as the 2nd light-shielding film 23, or is different is formed in parallel to the inside. The data-line drive circuit 101 and the external circuit connection terminal 102 which drive data-line 6a by supplying a picture signal to data-line 6a to predetermined timing are prepared in the field of the outside of a sealant 52 along with one side of the TFT array substrate 10, and the scanning-line drive circuit 104 which drives scanning-line 3a is formed along with two sides which adjoin this one side by supplying a scan signal to

scanning-line 3a to predetermined timing. If the scan signal delay supplied to scanning-line 3a does not become a problem, the thing only with one side sufficient [the scanning-line drive circuit 104] cannot be overemphasized. Moreover, the data-line drive circuit 101 may be arranged on both sides along the side of an image display field. For example, the data line of an odd number train supplies a picture signal from the data-line drive circuit arranged along one side of an image display field, and you may make it the data line of an even number train supply a picture signal from the data-line drive circuit arranged along the side of the opposite side of said image display field. Thus, if it is made to drive the data line in the shape of a ctenidium, since the occupancy area of a data-line drive circuit is extensible, it becomes possible to constitute a complicated circuit. Furthermore, two or more wiring 105 for connecting between the scanning-line drive circuits 104 established in the both sides of an image display field is formed in one side in which the TFT array substrate 10 remains. Moreover, in at least one place of the corner section of the opposite substrate 20, the flow material 106 for taking an electric flow between the TFT array substrate 10 and the opposite substrate 20 is formed. And as shown in drawing 17 , the opposite substrate 20 with the almost same profile as the sealant 52 shown in drawing 16 has fixed to the TFT array substrate 10 by the sealant 52 concerned. In addition, on the TFT array substrate 10, the inspection circuit for inspecting the sampling circuit which impresses a picture signal to two or more data-line 6a to predetermined timing, the precharge circuit which precedes the precharge signal of a predetermined voltage level with a picture signal, and supplies it to two or more data-line 6a respectively, the quality of the electro-optic device concerned at the manufacture middle or the time of shipment, a defect, etc. in addition to these data-line drive circuits 101 and scanning-line drive circuit 104 grade etc. may be formed. In addition, according to the gestalt of this operation, the 2nd light-shielding film 23 on the opposite substrate 20 can be easily removed by the application of an electro-optic device that what is necessary is just to form smaller than the protection-from-light field on the TFT array substrate 10.

[0144] You may make it connect with LSI for a drive mounted on the TAB (Tape Automated bonding) substrate instead of forming the data-line drive circuit 101 and the scanning-line drive circuit 104 on the TFT array substrate 10 electrically and mechanically through the anisotropy electric conduction film prepared in the periphery of the TFT array substrate 10 with each operation gestalt explained with reference to drawing 17 from drawing 1 above. Moreover, according to the exception of modes of operation, such as TN (Twisted Nematic) mode, VA (Vertically Aligned) mode, and PDLC (Polymer Dispersed Crystal) mode, and the no MARI White mode / NOMA reeve rack mode, a polarization film, a phase contrast film, the polarization version, etc. are respectively arranged in a predetermined direction at the side in which the outgoing radiation light of the side in which the incident light of the opposite substrate 20 carries out incidence, and the TFT array substrate 10 carries out outgoing radiation.

[0145] Since the electro-optic device in each operation gestalt explained above is applied to a projector, the electro-optic device of three sheets will be respectively used as a light valve for RGB, and incidence of the light of each color respectively decomposed through the dichroic mirror for RGB color separation will be respectively carried out to each light valve as incident light. Therefore, with each operation gestalt, the color filter is not prepared in the opposite substrate 20. However, the color filter of RGB may be formed in the predetermined field which counters pixel electrode 9a in which the 2nd light-shielding film 23 is not formed on the opposite substrate 20 with the protective coat. If it does in this way, the electro-optic device in each operation gestalt is applicable to the color electro-optic device of direct viewing types other than a liquid crystal projector, or a reflective mold. Furthermore, a micro lens may be formed so that it may correspond 1 pixel on [one] the opposite substrate 20. Or it is also possible to form a color filter layer in the bottom of pixel electrode 9a which counters RGB on the TFT array substrate 10 by a color resist etc. If it does in this way, a bright electro-optic device is realizable by improving the condensing effectiveness of incident light. Furthermore, the die clo IKKU filter which makes a RGB color using interference of light by depositing the interference layer to which the refractive index of many layers is different on the opposite substrate 20 again may be formed. According to this opposite substrate with a die clo ITSUKU filter, a brighter color electro-optic device is realizable.

[0146] Although [the electro-optic device in each operation gestalt explained above] incidence of the incident light is carried out from the opposite substrate 20 side as usual, since 1st light-shielding film 11a (or 11a') is prepared, incidence of the incident light is carried out from the TFT array substrate 10 side, and it may be made to carry out outgoing radiation from the opposite machine hill 20 side. That is, even if it attaches an electro-

optic device in a projector in this way, it can prevent light carrying out incidence to channel field 1a' of semi-conductor layer 1a, low concentration source field 1b, and low concentration drain field 1c, and it is possible to display a high-definition image. Although the polarizing plate with which AR (Anti Reflection) coat was carried out for acid resisting needs to be arranged separately or AR film needed to be stuck here in order to prevent the reflection by the side of the rear face of the TFT array substrate 10 conventionally With each operation gestalt, since [of the front face of the TFT array substrate 10, and semi-conductor layer 1a] 1st light-shielding film 11a (or 11a') is formed at least between channel field 1a', low concentration source field 1b, and low concentration drain field 1c, Such a polarizing plate and AR film by which AR coat was carried out are used, or the need of using the substrate which carried out AR processing of TFT array substrate 10 itself is lost. Therefore, according to each operation gestalt, ingredient cost can be reduced, and a contaminant, a blemish, etc. do not drop the yield at the time of polarizing plate attachment, and it is very advantageous. Moreover, since lightfastness is excellent, even if it uses the bright light source, or it carries out polarization conversion by the polarization beam splitter and it raises efficiency for light utilization, image quality degradation of the cross talk by light etc. is not produced.

[0147] Moreover, although explained as a switching element prepared in each pixel that it was the poly-Si TFT of a forward stagger mold or a coplanar mold, each operation gestalt is effective also to TFT of other formats, such as TFT of a reverse stagger mold, and an amorphous silicon TFT.

[0148] (Electronic equipment) Next, the gestalt of operation of electronic equipment equipped with the electro-optic device 100 explained to the detail above is explained with reference to drawing 20 from drawing 18 .

[0149] The outline configuration of the electronic equipment which equipped drawing 18 with the electro-optic device 100 in this way is shown first.

[0150] In drawing 18 , electronic equipment is constituted in preparation for the source 1000 of a display information output, the display information processing circuit 1002, the drive circuit 1004, an electro-optic device 100, and clock generation circuit 1008 list in the power circuit 1010. The source 1000 of a display information output outputs display information, such as a picture signal of a predetermined format, to the display information processing circuit 1002 based on the clock signal from the clock generation circuit 1008 including the tuning circuit which aligns and outputs memory, such as ROM (Read Only Memory), RAM (Random Access Memory), and an optical disk unit, and a picture signal. The display information processing circuit 1002 is constituted including various well-known processing circuits, such as magnification and a polarity-reversals circuit, a serial parallel conversion circuit, a rotation circuit, a gamma correction circuit, and a clamping circuit, carries out sequential generation of the digital signal from the display information inputted based on the clock signal, and outputs it to the drive circuit 1004 with a clock signal CLX. The drive circuit 1004 drives an electro-optic device 100. A power circuit 1010 supplies a predetermined power source to each above-mentioned circuit. In addition, on the TFT array substrate which constitutes an electro-optic device 100, the drive circuit 1004 may be carried and, in addition to this, the display information processing circuit 1002 may be carried.

[0151] Next, the example of the electronic equipment constituted in this way from drawing 19 by drawing 20 is shown respectively.

[0152] In drawing 19 , an example slack projector 1100 of electronic equipment prepares three light valves with which the drive circuit 1004 mentioned above contains the electro-optic device 100 carried on the TFT array substrate, and is constituted as a projector respectively used as light valves 100R, 100G, and 100B for RGB. In a projector 1100, if incident light is emitted from the lamp unit 1102 of sources of the white light, such as a metal halide lamp, it will be divided into parts for Mitsunari R, G, and B corresponding to the three primary colors of RGB with the mirror 1106 of three sheets, and the dichroic mirror 1108 of two sheets, and will be respectively led to the light valves 100R, 100G, and 100B corresponding to each color. Under the present circumstances, especially B light is drawn through the relay lens system 1121 which consists of the incidence lens 1122, a relay lens 1123, and an outgoing radiation lens 1124, in order to prevent the optical loss by the long optical path. And after a part for Mitsunari corresponding to the three primary colors respectively modulated with light valves 100R, 100G, and 100B is again compounded with a dichroic prism 1112, it is projected on it by the screen 1120 as a color picture through a projector lens 1114.

[0153] In drawing 20 , the electro-optic device 100 mentioned above is formed in the top covering case, and other personal computers 1200 of the laptop type corresponding to example slack multimedia of electronic

equipment (PC) are equipped with the body 1204 with which the keyboard 1202 was incorporated while they hold CPU, memory, a modem, etc. further.

[0154] ****** equipped with the video tape recorder of a liquid crystal television, a viewfinder mold, or a monitor direct viewing type, the car navigation equipment, the electronic notebook, the calculator, the word processor, the engineering workstation (EWS), the cellular phone, the TV phone, POS terminal, and touch panel other than electronic equipment which were explained with reference to drawing 20 from drawing 19 above etc. is mentioned as an example of the electronic equipment shown in drawing 18 .

[0155] As explained above, according to the gestalt of this operation, various kinds of electronic equipment equipped with the electro-optic device in which high-definition image display with high manufacture effectiveness is possible is realizable.

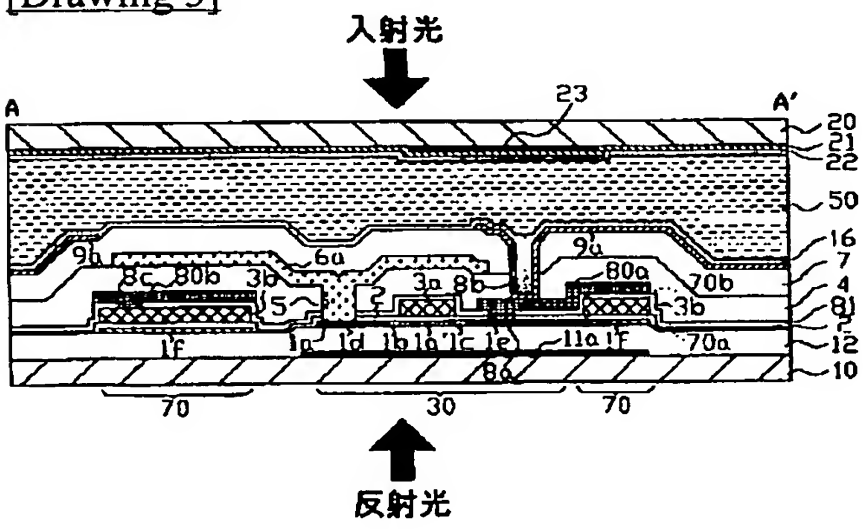
[Translation done.]

* NOTICES *

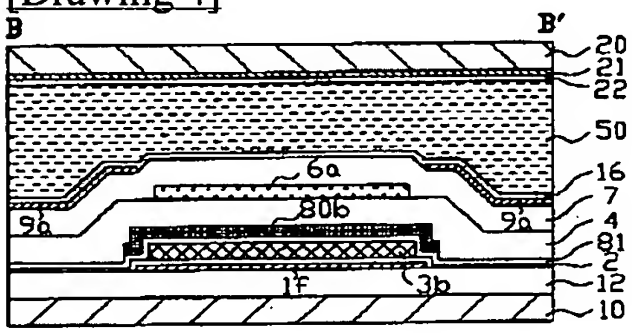
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

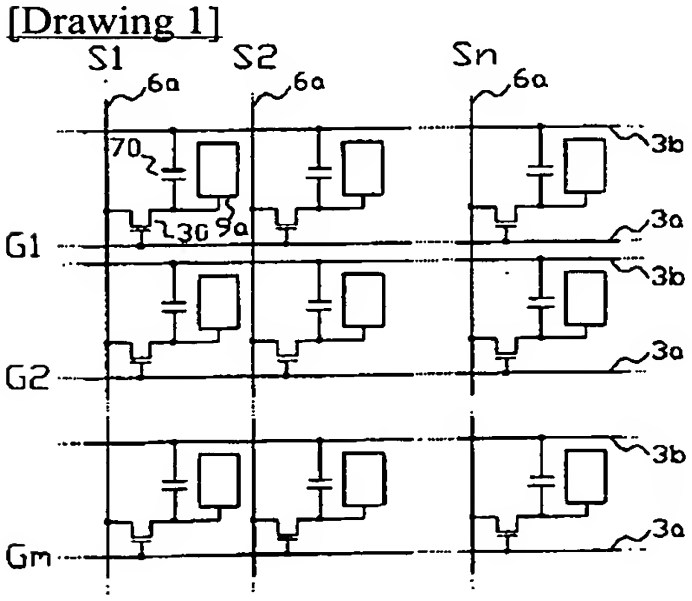
[Drawing 3]



[Drawing 4]



[Drawing 1]



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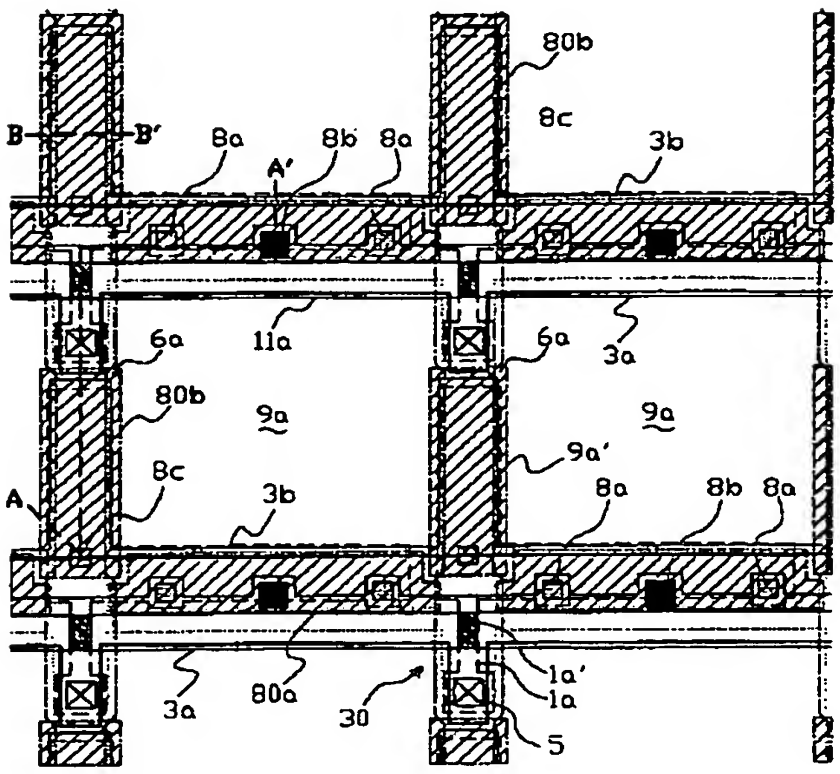
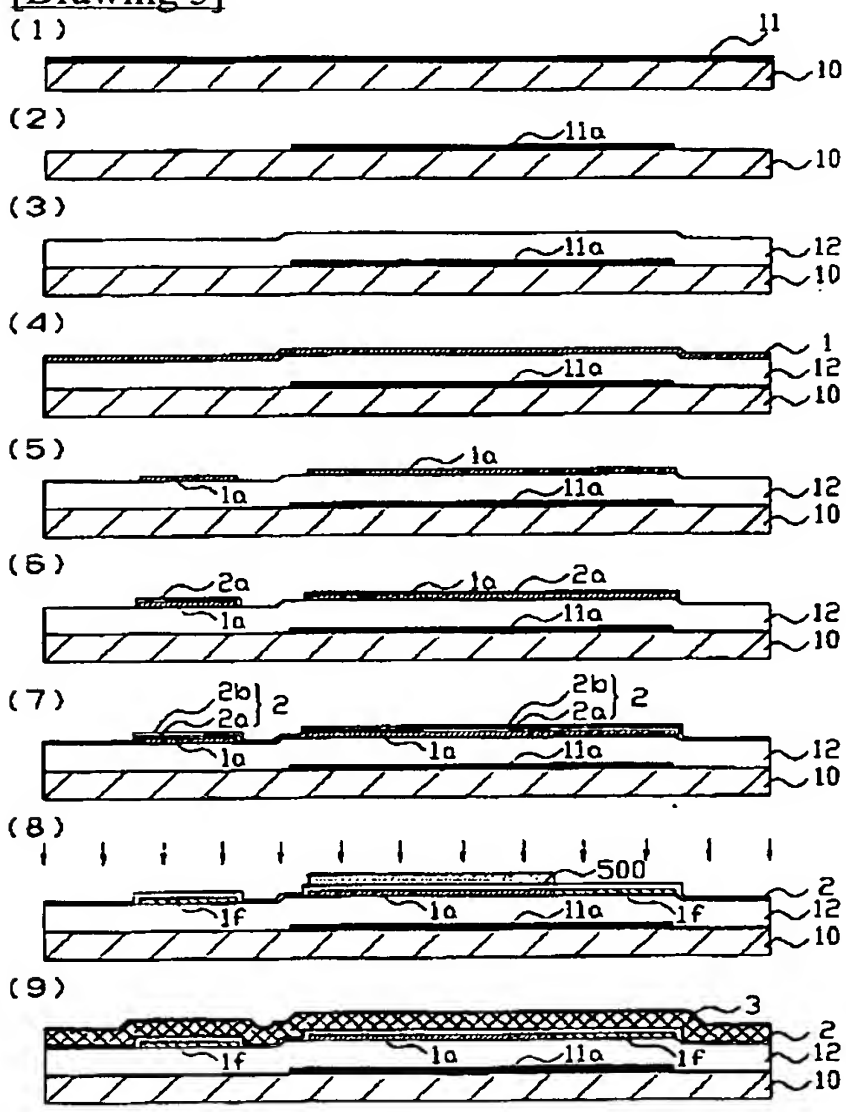


[Drawing 5]



[Drawing 6]

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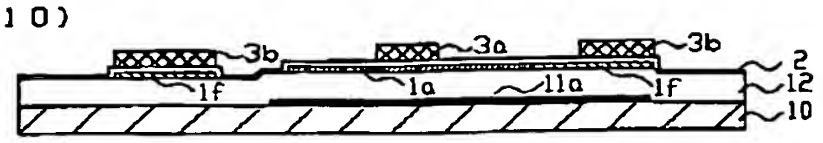

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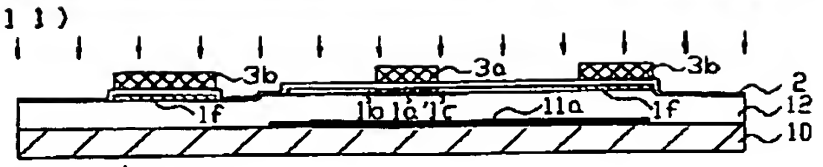

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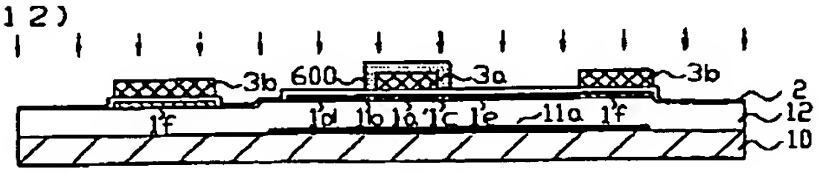

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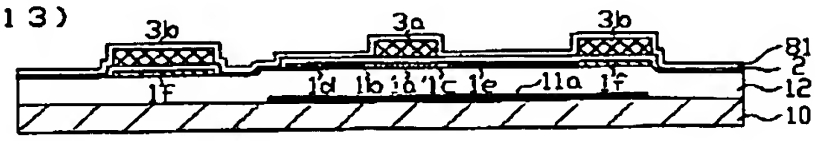

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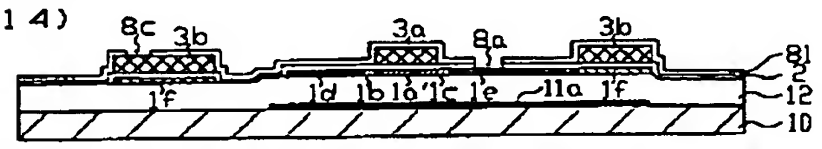

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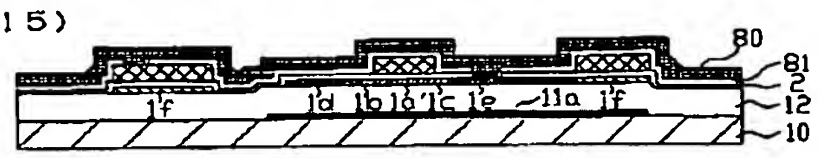

[Drawing 7]

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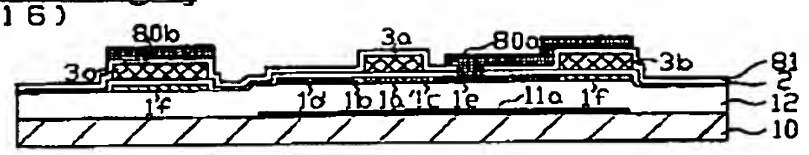

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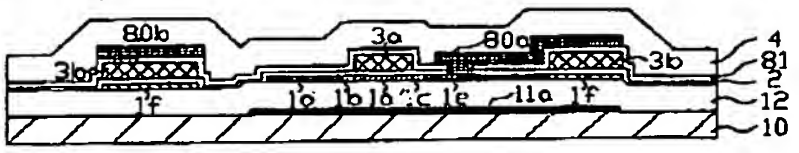

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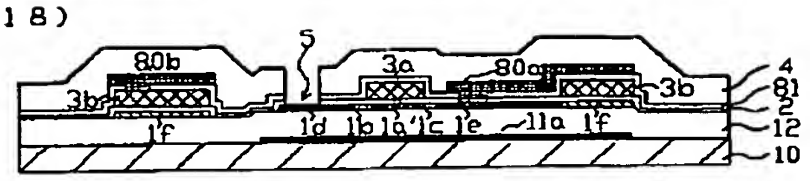

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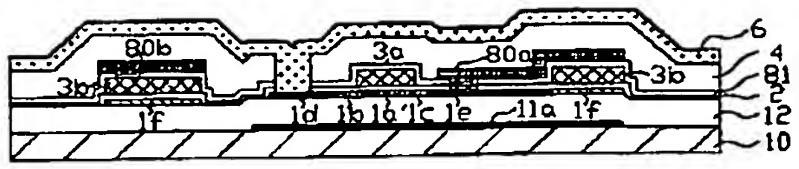

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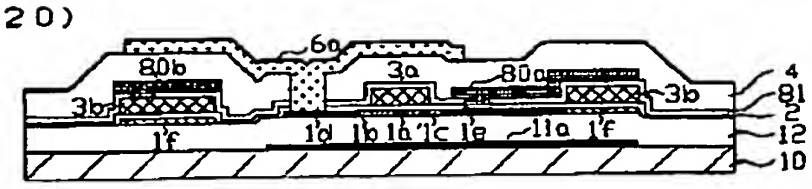

[Drawing 8]

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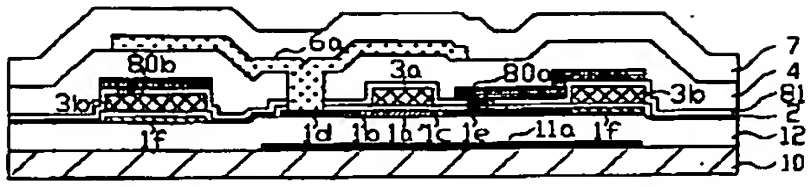

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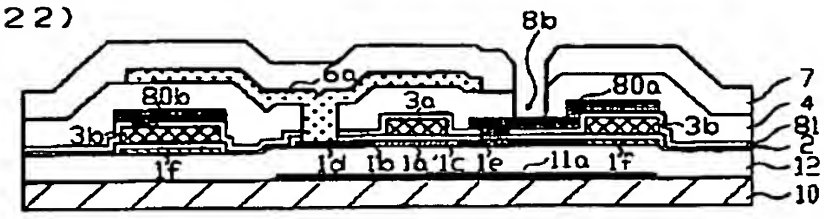

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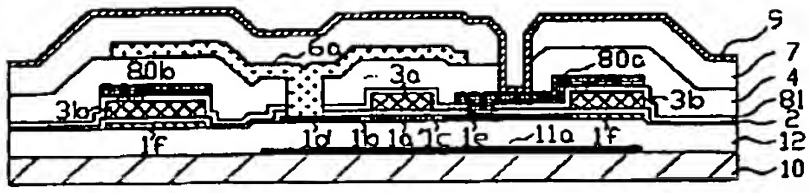

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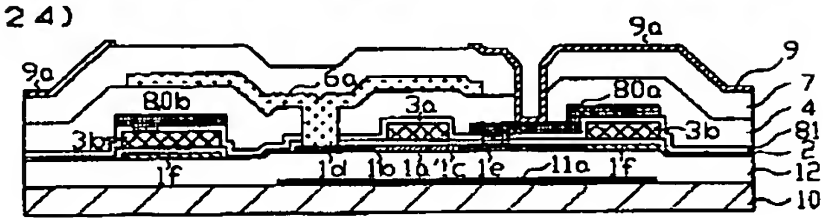

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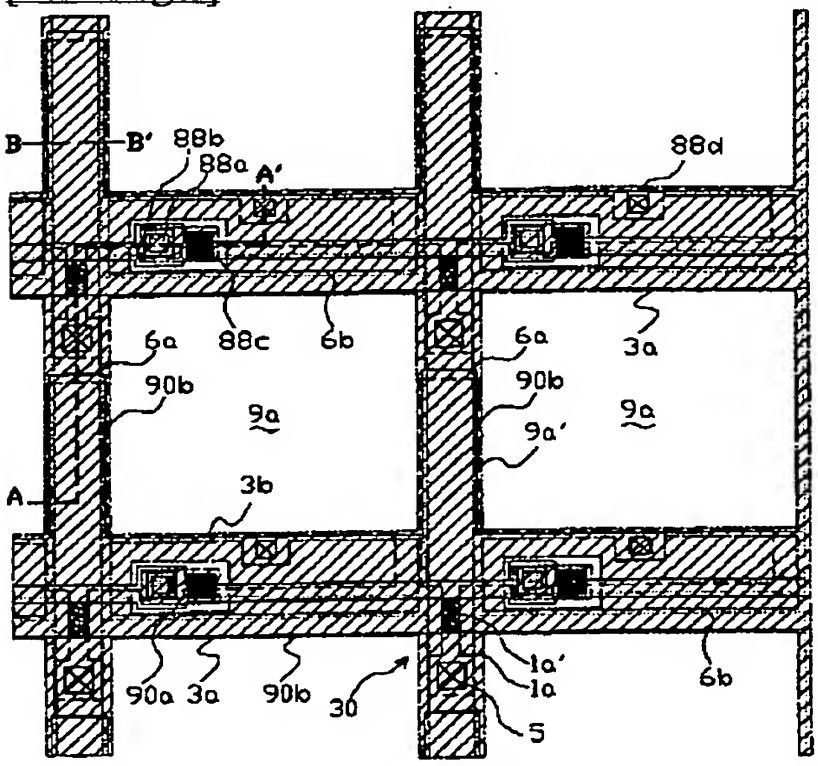
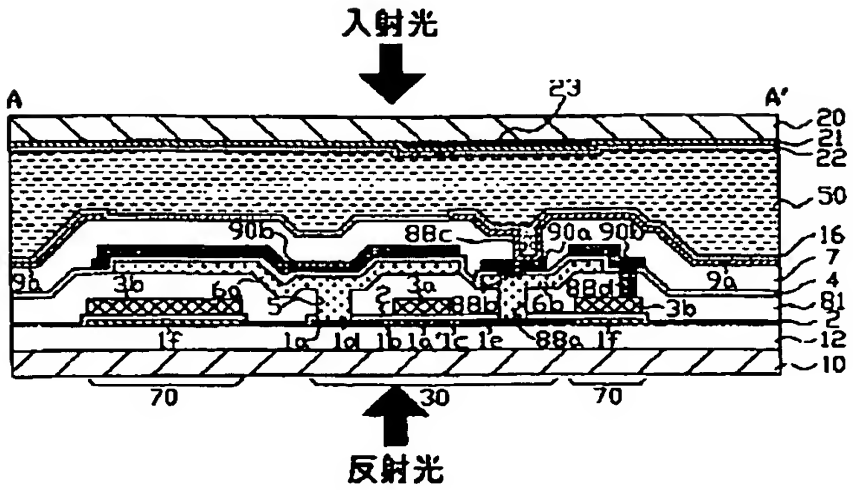


[Drawing 10]



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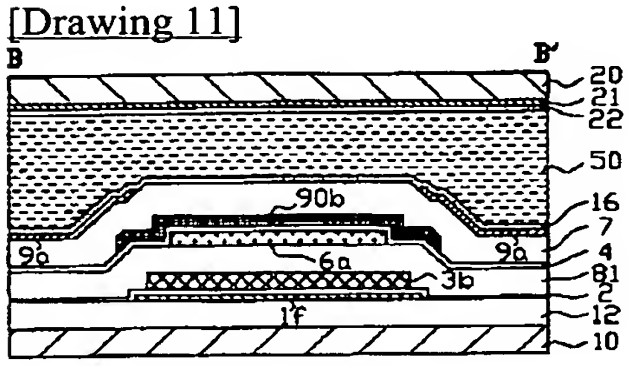

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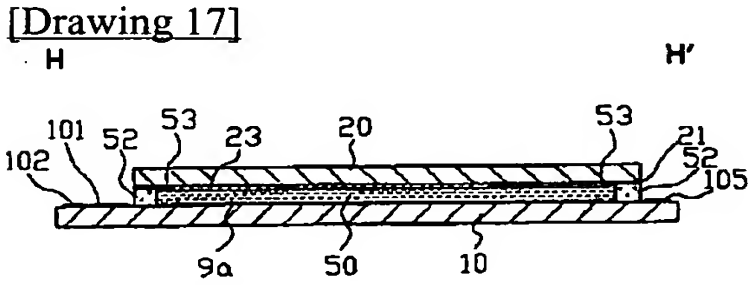
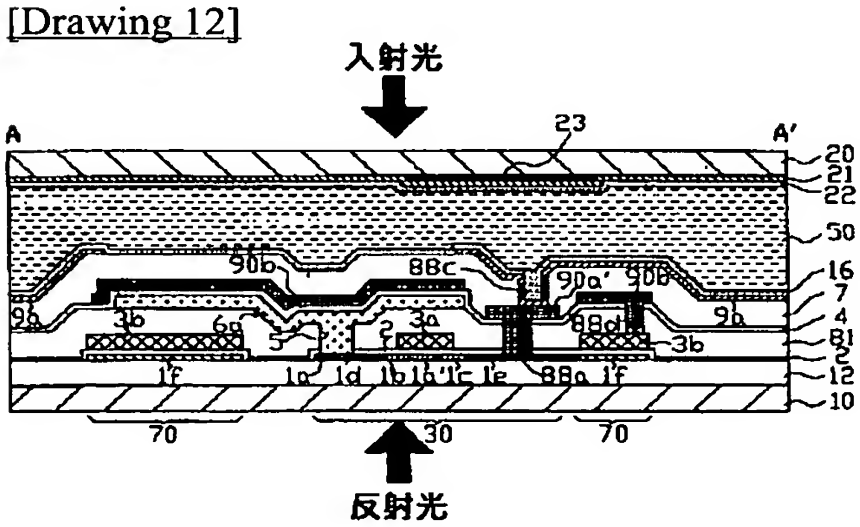


[Drawing 12]



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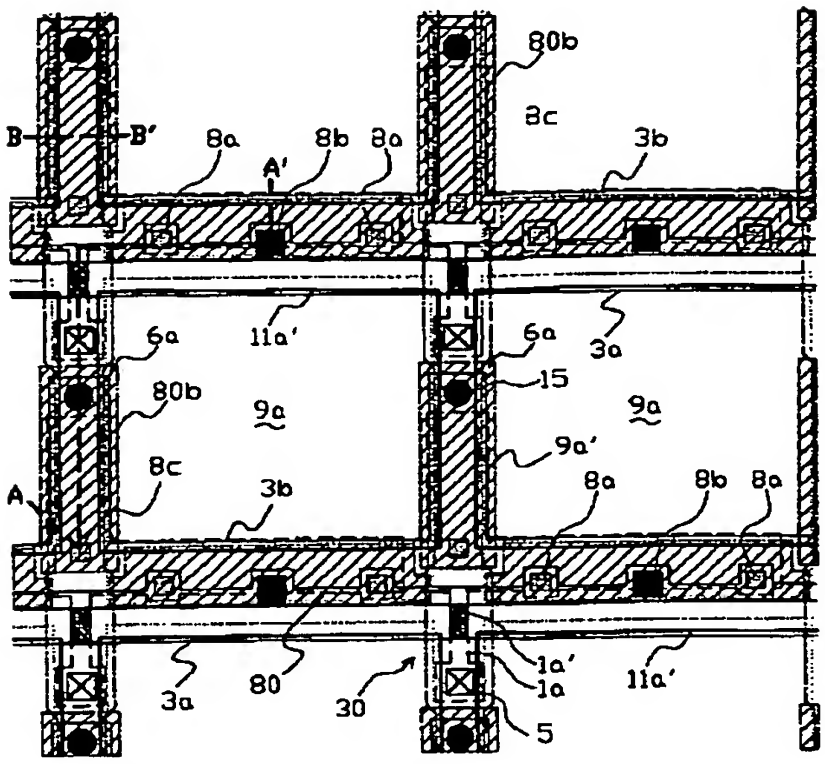

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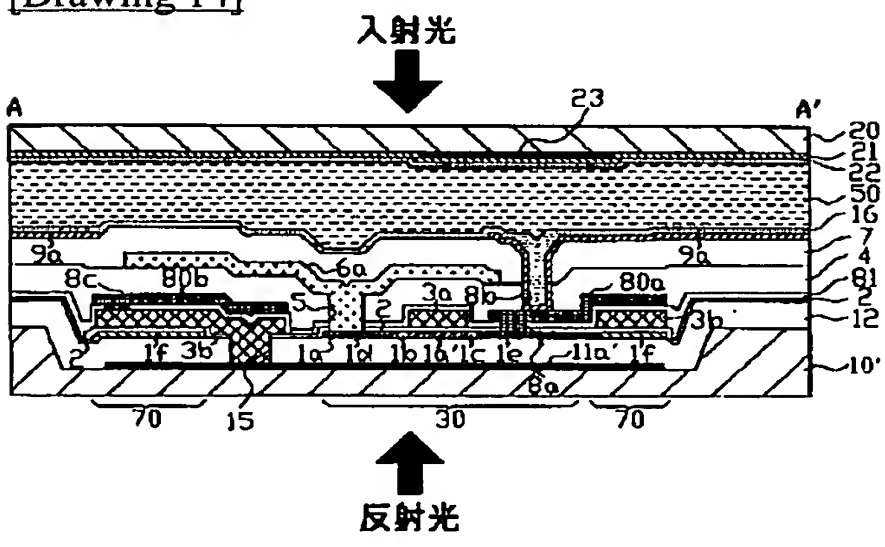

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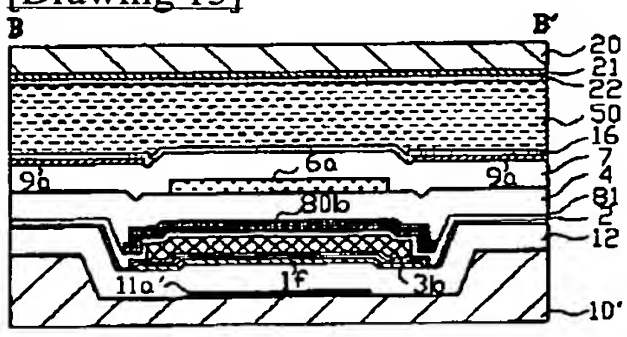
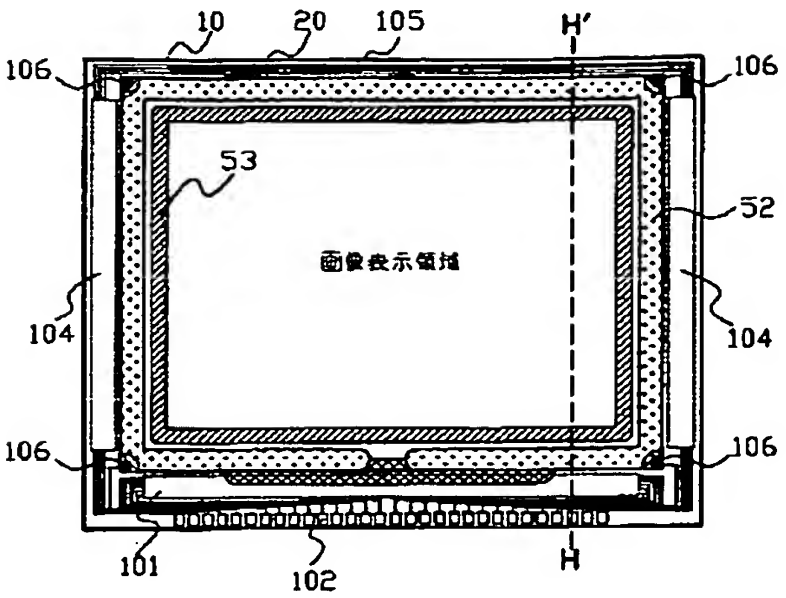
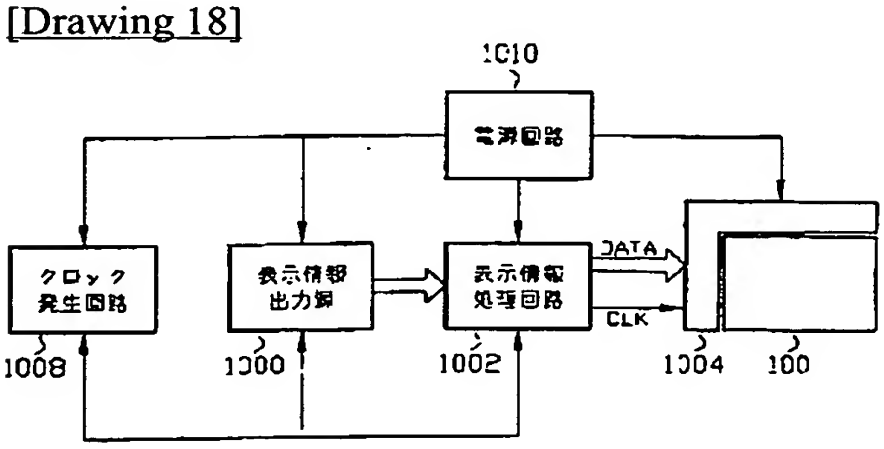


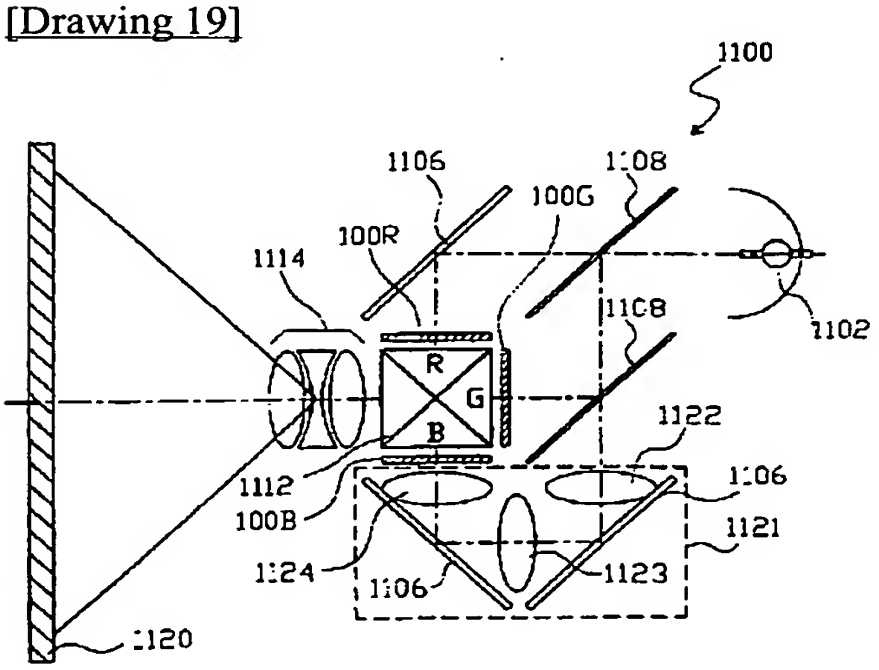
[Drawing 16]



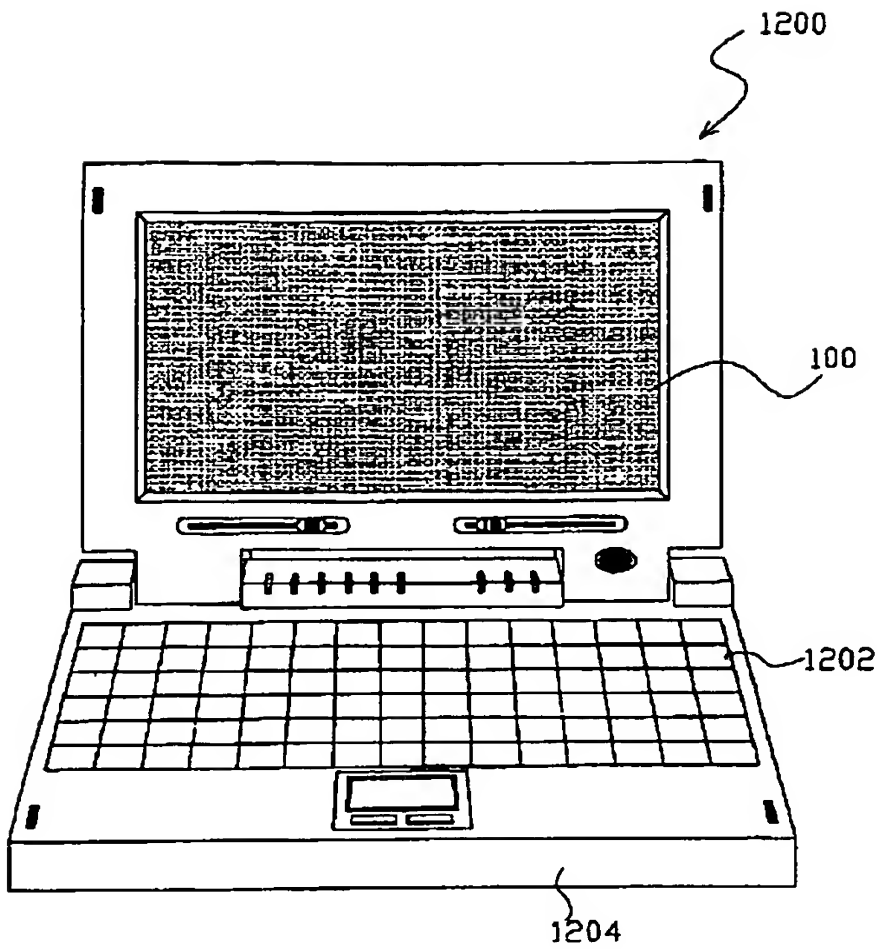
[Drawing 18]



[Drawing 19]



[Drawing 20]



[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CORRECTION OR AMENDMENT

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[Procedure amendment 1]
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[Item(s) to be Amended] The name of invention
[Method of Amendment] Modification
[The contents of amendment]
[Title of the Invention] An electro-optic device and electronic equipment
[Procedure amendment 2]
[Document to be Amended] Specification
[Item(s) to be Amended] Claim
[Method of Amendment] Modification
[The contents of amendment]
[Claim(s)]
[Claim 1]
It is the electro-optic device which has the thin film transistor arranged at the substrate corresponding to the crossover of two or more scanning lines, two or more data lines, and the said each scanning line and said each data line, and a pixel electrode,
The 1st junction conductive layer which was electrically connected to the semi-conductor layer of said thin film transistor, and was formed by the same film as said data line,

The light-shielding film which is formed in the upper layer and specifies a pixel opening field partially at least from said data line,
The field where said light-shielding film was removed partially,
The 2nd junction conductive layer which was formed by the same film as said light-shielding film, was formed in the field to which said light-shielding film was removed partially, and was electrically connected with said 1st junction conductive layer,
The electro-optic device characterized by providing the pixel electrode electrically connected to said 2nd junction conductive layer.
[Claim 2]
It is the electro-optic device which has the thin film transistor arranged at the substrate corresponding to the crossover of two or more scanning lines, two or more data lines, and the said each scanning line and said each data line, and a pixel electrode,
The light-shielding film which is formed in the upper layer and specifies a pixel opening field partially at least from said data line,
The field where said light-shielding film was removed partially,
The junction conductive layer which was formed by the same film as said light-shielding film, was formed in the field to which said light-shielding film was removed partially, and was electrically connected with the semi-conductor layer of said thin film transistor,
The electro-optic device characterized by providing the pixel electrode electrically connected to said junction conductive layer.
[Claim 3]
The field where said light-shielding film was removed partially is an electro-optic device according to claim 1 or 2 characterized by being formed in the field of the light-shielding film between said adjoining data lines.
[Claim 4]
An electro-optic device given in any 1 term of claim 1 characterized by having the 1st storage capacitance electrode formed in the drain field of said semi-conductor layer, and the 2nd storage capacitance electrode which is formed by the same film as the gate electrode of said thin film transistor, and laps with said 1st storage capacitance electrode thru/or claim 3.
[Claim 5]
Said drain field is an electro-optic device according to claim 4 characterized by being formed along with said scanning line.
[Claim 6]
Said drain field is an electro-optic device according to claim 4 or 5 characterized by being formed along with said data line.
[Claim 7]
Said light-shielding film is an electro-optic device given in any 1 term of claim 4 which is constant potential and is characterized by connecting said 2nd storage capacitance electrode with said light-shielding film electrically thru/or claim 6.
[Claim 8]
The electrical installation of said light-shielding film and said 2nd storage capacitance electrode is an electro-optic device according to claim 7 characterized by being formed in the field of the light-shielding film between said adjoining data lines.
[Claim 9]
Electronic equipment characterized by having the electro-optic device of a publication in any 1 term of claim 1 to claim 8.
[Procedure amendment 3]
[Document to be Amended] Specification
[Item(s) to be Amended] 0009
[Method of Amendment] Modification
[The contents of amendment]
[0009]
[Means for Solving the Problem]
In order that the electro-optic device of this invention may solve the above-mentioned technical problem, this

invention is characterized by the electro-optic device which has the thin film transistor arranged at the substrate corresponding to the crossover of two or more scanning lines, two or more data lines, and the said each scanning line and said each data line and a pixel electrode possessing the following. The 1st junction conductive layer which was electrically connected to the semi-conductor layer of said thin film transistor, and was formed by the same film as said data line The light-shielding film which is formed in the upper layer and specifies a pixel opening field partially at least from said data line The field where said light-shielding film was removed partially The pixel electrode electrically connected to the 2nd junction conductive layer which was formed by the same film as said light-shielding film, was formed in the field to which said light-shielding film was removed partially, and was electrically connected with said 1st junction conductive layer, and said 2nd junction conductive layer

Moreover, this invention is characterized by the electro-optic device which has the thin film transistor arranged at the substrate corresponding to the crossover of two or more scanning lines, two or more data lines, and the said each scanning line and said each data line and a pixel electrode possessing the following, in order that the electro-optic device of this invention may solve the above-mentioned technical problem. The light-shielding film which is formed in the upper layer and specifies a pixel opening field partially at least from said data line The field where said light-shielding film was removed partially The junction conductive layer which was formed by the same film as said light-shielding film, was formed in the field to which said light-shielding film was removed partially, and was electrically connected with the semi-conductor layer of said thin film transistor The pixel electrode electrically connected to said junction conductive layer

Moreover, it is characterized by equipping this invention with the following. To a substrate, they are two or more scanning lines. Two or more data lines The thin film transistor and pixel electrode which have been arranged corresponding to the crossover of said each scanning line and each of said data line The 2nd conductive layer which intervened between the semi-conductor layer which constitutes the source and the drain field of said thin film transistor, and said pixel electrode, consisted of the same film as the 1st conductive layer of the protection-from-light nature which was electrically connected with said semi-conductor layer, and was electrically connected with said pixel electrode, and said 1st conductive layer, saw superficially, and has lapped with said data line partially at least

[Procedure amendment 4]

[Document to be Amended] Specification

[Item(s) to be Amended] 0062

[Method of Amendment] Modification

[The contents of amendment]

[0062]

The scanning line of plurality [approach / of the electro-optic device of this invention / manufacture / substrate], and two or more data lines, In the manufacture approach of an electro-optic device of having the thin film transistor connected to said each scanning line and said each data line, and the pixel electrode to which said thin film transistor was connected The process which forms the semi-conductor layer used as a source field, a channel field, and a drain field in said substrate, The process which forms an insulating thin film on said semi-conductor layer, and the process which forms one electrode of the scanning line and storage capacitance in the predetermined field on said insulating thin film, The process which forms the 1st interlayer insulation film on said scanning line and one [said] electrode, The process which punctures ** 1 contact hole which leads to said semi-conductor layer to said insulating thin film and said 1st interlayer insulation film, So that it may connect with said semi-conductor layer electrically through said 1st contact hole on said 2nd insulator layer The 1st conductive layer of protection-from-light nature, The process which forms the 2nd conductive layer from the same film as said 1st conductive layer, and the process which forms the 2nd interlayer insulation film on said 1st conductive layer and said 2nd conductive layer, The process which forms the data line on said 2nd **********, and the process which forms the 3rd interlayer insulation film on said data line, The process which punctures the 2nd contact hole which leads to said 2nd interlayer insulation film and said 3rd interlayer insulation film at said 1st conductive layer, It has the process which forms a pixel electrode so that it may connect with said 1st conductive layer electrically through said 2nd contact hole, and said 2nd conductive layer is formed so that it may see superficially and may lap with said data line partially at least.

[Procedure amendment 5]

[Document to be Amended] Specification

[Item(s) to be Amended] 0063
[Method of Amendment] Modification
[The contents of amendment]
[0063]
According to the manufacture approach of the electro-optic device of this invention, laminating formation of the 1st interlayer insulation film is carried out in this order in one electrode list of a semi-conductor layer, an insulating thin film, the scanning line, and storage capacitance at a substrate. Next, the 1st contact hole which leads to a semi-conductor layer is punctured by an insulating thin film and the 1st interlayer insulation film, and the 1st conductive layer of protection-from-light nature is formed so that it may connect with a semi-conductor layer electrically through this 1st contact hole. The 2nd conductive layer is formed so that it may be partially arranged at least in the gap of the field where it sees to coincidence superficially and a pixel electrode is formed in it from the same film as this 1st conductive layer. Then, laminating formation of the 2nd interlayer insulation film, the data line, and the 3rd interlayer insulation film is carried out in this order. Next, the 2nd contact hole which leads to the 1st conductive layer is punctured, and pixel ionization formation is carried out so that it may connect with the 1st conductive layer electrically through this 2nd contact hole. Therefore, the electro-optic device of this invention which has the configuration which forms the 1st and 2nd conductive layers as a layer near a substrate, and relays a pixel electrode and a semi-conductor layer by the 2nd conductive layer through two contact holes rather than the data line mentioned above can be manufactured comparatively easily. Since the 1st conductive layer and the 2nd conductive layer are especially formed from the same film, low cost-ization can be attained in the simplification list of a manufacture process.
[Procedure amendment 6]
[Document to be Amended] Specification
[Item(s) to be Amended] 0064
[Method of Amendment] Modification
[The contents of amendment]
[0064]
In the mode of 1 of the manufacture approach of said electro-optic device of this invention In the process which forms said data line after the process which forms said 2nd interlayer insulation film, including further the process which punctures the 3rd contact hole which leads to said semi-conductor layer to said 2nd interlayer insulation film In the process which forms said data line so that it may connect with said semi-conductor layer electrically through said 3rd contact hole, and punctures said 1st contact hole In the process which punctures the 4th contact hole which leads to one electrode of said storage capacitance to said 1st interlayer insulation film at the same time it punctures said 1st contact hole, and forms said 2nd conductive layer Said 2nd conductive layer is formed so that it may connect with one electrode of said storage capacitance electrically through said 4th contact hole.
[Procedure amendment 7]
[Document to be Amended] Specification
[Item(s) to be Amended] 0066
[Method of Amendment] Modification
[The contents of amendment]
[0066]
This invention is characterized by the manufacture approach of an electro-optic device that the manufacture approach of other electro-optic devices of this invention has the pixel electrode by which the thin film transistor connected to the scanning line, two or more data lines, and two or more of said each scanning line and said each data line and said thin film transistor were connected to the substrate possessing the following. The process which forms the semi-conductor layer used as a source field, a channel field, and a drain field in said substrate The process which forms an insulating thin film on said semi-conductor layer The process which forms one electrode of the scanning line and storage capacitance on said insulating thin film The process which forms the 1st interlayer insulation film on one electrode of said scanning line and storage capacitance, The process which punctures the 1st contact hole which leads to said semi-conductor layer to said 1st interlayer insulation film, The process which forms a junction conductive layer from the same film as said data line so that it may connect with said semi-conductor layer electrically through said 1st contact hole at the same time it forms the data line on said 1st interlayer insulation film, The process which forms the 2nd interlayer insulation film on said data

line and said junction conductive layer, The process which punctures the 2nd contact hole which leads to said 2nd interlayer insulation film at said junction conductive layer, At the same time it forms the 1st conductive layer of protection-from-light nature so that it may connect with said junction conductive layer electrically through said 2nd contact hole on said 2nd interlayer insulation film The process which forms the 2nd conductive layer which consists of the same film as said 1st conductive layer so that it may lap with said data line superficially, The process which forms the 3rd interlayer insulation film on said 1st conductive layer and said 2nd conductive layer, The process which punctures the 3rd contact hole which leads to said 3rd interlayer insulation film at said 1st conductive layer, and the process which forms a pixel electrode so that it may connect electrically through said 3rd contact hole at said 1st conductive layer

[Procedure amendment 8]
[Document to be Amended] Specification
[Item(s) to be Amended] 0067
[Method of Amendment] Modification
[The contents of amendment]
[0067]
According to the manufacture approach of the electro-optic device of this invention, laminating formation of the 1st interlayer insulation film is carried out in this order in one electrode list of a semi-conductor layer, an insulating thin film, the scanning line, and storage capacitance at a substrate. Next, the contact hole which leads to a semi-conductor layer is punctured, and a junction conductive layer is formed from the same film as the data line so that it may connect with a semi-conductor layer electrically, at the same time the data line is formed. Next, after the 2nd interlayer insulation film is formed, the contact hole which leads to a junction conductive layer is punctured, and the 1st conductive layer of protection-from-light nature is formed so that it may connect with a junction conductive layer electrically. It can come, simultaneously the 2nd conductive layer is formed from the same film as the 1st conductive layer. Then, the 3rd interlayer insulation film is formed, the contact hole which leads to the 1st conductive layer is punctured, and a pixel electrode is formed so that it may connect with the 1st conductive layer electrically. Therefore, as the layer further than the data line from a substrate, i.e., the upper layer, while forming a junction conductive layer as a conductive layer which consists of the same film as the data line mentioned above, the 1st conductive layer is formed, and while relaying a pixel electrode and a semi-conductor layer by the junction conductive layer and the 1st conductive layer through three contact holes, the electro-optic device of this invention which has the configuration which specifies a pixel opening field by the 2nd conductive layer can be manufactured comparatively easily. Since the 1st conductive layer and the 2nd conductive layer are especially formed from the same film, low cost-ization can be attained in the simplification list of a manufacture process.

[Procedure amendment 9]
[Document to be Amended] Specification
[Item(s) to be Amended] 0068
[Method of Amendment] Modification
[The contents of amendment]
[0068]
In the mode of 1 of the manufacture approach of said electro-optic device of this invention In the process which forms said data line after the process which forms said 1st interlayer insulation film, including further the process which punctures the 4th contact hole which leads to said semi-conductor layer to said 1st interlayer insulation film In the process which forms said data line so that it may connect with said semi-conductor layer electrically through said 4th contact hole, and punctures said 2nd contact hole In the process which punctures the 5th contact hole which leads to one electrode of said storage capacitance to said 1st interlayer insulation film and said 2nd interlayer insulation film at the same time it punctures said 2nd contact hole, and forms said 2nd conductive layer Said 2nd conductive layer is formed so that it may connect with one electrode of said storage capacitance electrically through said 5th contact hole.

[Translation done.]

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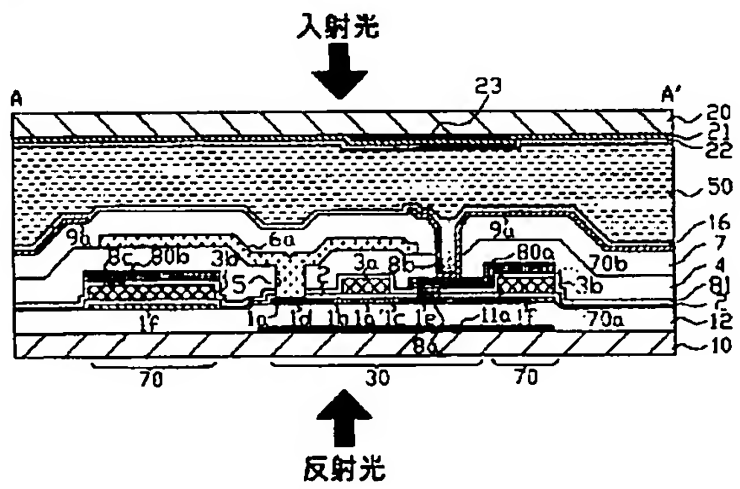
最終頁に続く

(54)【発明の名称】　電気光学装置及びその製造方法並びに電子機器

(57)【要約】
【課題】　ＴＦＴアクティブマトリクス駆動方式の電気光学装置において、比較的簡単な構成で、画素電極と半導体層とを中継しつつ画素開口率を高め、高品位の画像表示を可能とする。
【解決手段】　画素電極及びＴＦＴ間は、第１バリア層（８０a）を中継してコンタクトホール（８a）及びコンタクトホール（８ｂ）により電気接続される。第２バリア層（８０ｂ）は、データ線（６a）より幅広に設けられており、その一端が画素電極（９a）に重なって、画素開口領域を規定する。



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【特許請求の範囲】

【請求項１】　基板に、

複数の走査線と、

複数のデータ線と、

前記各走査線及び前記各データ線の交差に対応して配置された薄膜トランジスタと画素電極と、

前記薄膜トランジスタのソース及びドレイン領域を構成する半導体層と前記画素電極との間に介在し、前記半導体層と電気的に接続され且つ前記画素電極と電気的に接続された遮光性の第１導電層と、

前記第１導電層と同一膜からなり、平面的に見て前記データ線に少なくとも部分的に重なっている第２導電層とを備えたことを特徴とする電気光学装置。

【請求項２】　前記第２導電層は平面的に見て少なくとも部分的に前記画素電極に重なっていることを特徴とする請求項１に記載の電気光学装置。

【請求項３】　前記第１導電層は、前記半導体層と第１コンタクトホールを介して電気的に接続され且つ前記画素電極と第２コンタクトホールを介して電気的に接続されたことを特徴とする請求項１又は２に記載の電気光学装置。

【請求項４】　前記データ線は、前記半導体層と第３コンタクトホールを介して電気的に接続されたことを特徴とする請求項１から３のいずれか一項に記載の電気光学装置。

【請求項５】　前記データ線は、平面的に見て前記画素電極に少なくとも部分的に重ならないことを特徴とする請求項１から４のいずれか一項に記載の電気光学装置。

【請求項６】　前記第２導電層は、定電位線に電気的に接続されていることを特徴とする請求項１から５のいずれか一項に記載の電気光学装置。

【請求項７】　前記半導体層のうち少なくともチャネル領域の前記基板側に下地絶縁膜を介して形成された遮光膜を更に備えたことを特徴とする請求項１から６のいずれか一項に記載の電気光学装置。

【請求項８】　前記第１導電層及び前記第２導電層は、高融点金属を含むことを特徴とする請求項１から７のいずれか肘項に記載の電気光学装置。

【請求項９】　前記第２導電層と前記データ線とは、層間絶縁膜を介して少なくとも部分的に対向配置されたことを特徴とする請求項１から８のいずれか一項に記載の電気光学装置。

【請求項１０】　前記画素電極に接続された蓄積容量を更に備えたことを特徴とする請求項１から９のいずれか一項に記載の電気光学装置。

【請求項１１】　前記第１導電層及び前記第２導電層は、前記走査線及び前記蓄積容量の一方の電極上に絶縁膜を介して設けられていることを特徴とする請求項１０に記載の電気光学装置。

【請求項１２】　前記半導体層の一部からなる第１蓄積

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容量電極と前記蓄積容量の一方の電極である第２蓄積容量電極とが第１誘電体膜を介して対向配置され、前記第２蓄積容量電極と前記第１導電層の一部からなる第３蓄積容量電極とが第２誘電体膜を介して対向配置されて前記蓄積容量が形成されていることを特徴とする請求項１１に記載の電気光学装置。

【請求項１３】　前記第２導電層は、前記第２蓄積容量電極に接続されたことを特徴とする請求項１０から１２のいずれか一項に記載の電気光学装置。

【請求項１４】　前記第２導電層は、第４コンタクトホールを介して前記第２蓄積容量電極に電気的に接続されており、

前記第４コンタクトホールは、前記第１コンタクトホールを開孔する工程と同一工程により開孔されていることを特徴とする請求項１３に記載の電気光学装置。

【請求項１５】　前記第２蓄積容量電極は延設されて容量線であることを特徴とする請求項１２に記載の電気光学装置。

【請求項１６】　前記第２蓄積容量電極は前記遮光膜と接続されてなることを特徴とする請求項１３に記載の電気光学装置。

【請求項１７】　前記遮光膜は容量線を兼ね、前記第２蓄積容量電極は、前記基板上における平面形状が相隣接するデータ線間を前記走査線に沿って伸び、各画素電極毎に島状に構成されているとともに、前記遮光膜に接続されてなることを特徴とする請求項１６に記載の電気光学装置。

【請求項１８】　前記遮光膜は、前記第４コンタクトホールとは異なる平面位置に開孔された第５コンタクトホールを介して前記容量線に電気的に接続されていることを特徴とする請求項１５に記載の電気光学装置。

【請求項１９】　前記第２導電層と前記遮光膜とは前記第２蓄積容量電極を介して電気的に接続されてなり、前記第２導電層と前記遮光膜とは隣接する画素電極に接続されてなることを特徴とする請求項１０から１８のいずれか一項に記載の電気光学装置。

【請求項２０】　前記第１導電層及び前記第２導電層は、前記データ線よりも下層に設けられていることを特徴とする請求項１から１９のいずれか一項に記載の電気光学装置。

【請求項２１】　前記第２導電層は、平面的に見て島状に設けられており、画素開口領域のうち前記データ線に沿った領域を少なくとも部分的に規定することを特徴とする詣求項１から２０のいずれか一項に記載の電気光学装置。

【請求項２２】　前記第１導電層及び前記第２導電層は、前記データ線よりも上層に設けられていることを特徴とする請求項１から１０のいずれか一項に記載の電気光学装置。

【請求項２３】　前記第２導電層は、平面的に見て前記

第１導電層が存在する領域を除き格子状に設けられており、画素開口領域の前記データ線及び前記走査線に沿った領域を規定することを特徴とする請求項２２に記載の電気光学装置。

【請求項２４】　前記半導体層と前記第１導電層とは前記データ線と同一膜からなる中継導電層を介して接続されていることを特徴とする請求項２２又は２３に記載の電気光学装置。

【請求項２５】　前記画素電極に接続された蓄積容量を有し、

前記データ線は前記蓄積容量の一方の電極と前記第２導電層との間に層間絶縁膜を介して扶持されたことを特徴とする請求項２４に記載の電気光学装置。

【請求項２６】　基板に複数の走査線と、複数のデータ線と、前記各走査線と前記各データ線に接続された薄膜トランジスタと、前記薄膜トランジスタの接続された画素電極とを有する電気光学装置の製造方法において、

前記基板にソース領域、チャネル領域及びドレイン領域となる半導体層を形成する工程と、

前記半導体層上に絶縁薄膜を形成する工程と、

前記絶縁薄膜上に走査線及び蓄積容量の一方の電極を形成する工程と、

前記走査線及び前記一方の電極上に第１層間絶縁膜を形成する工程と、

前記絶縁薄膜及び前記第１層間絶縁膜に前記半導体層に通じる第１コンタクトホールを開孔する工程と、

前記第１層間絶縁膜上に、前記第１コンタクトホールを介して前記半導体層に電気的に接続されるように遮光性の第１導電層と前記第１導電層と同一膜から第２導電層を形成する工程と、

前記第１導電層及び前記第２導電層上に第２層間絶縁膜を形成する工程と、

前記第２層間絶縁膜上にデータ線を形成する工程と、

前記データ線上に第３層間絶縁膜を形成する工程と、

前記第２層間絶縁膜及び前記第３層間絶縁膜に前記第１導電層に通じる第２コンタクトホールを開孔する工程と、

前記第２コンタクトホールを介して前記第１導電層に電気的に接続されるように画素電極を形成する工程とを有し、前記第２導電層は、平面的に見て前記データ線に少なくとも部分的に重なるように形成されていることを特徴とする電気光学装置の製造方法。

【請求項２７】　前記第２層間絶縁膜を形成する工程の後に、前記第２層間絶縁膜に前記半導体層に通じる第３コンタクトホールを開孔する工程を更に含み、前記データ線を形成する工程において、前記第３コンタクトホールを介して前記半導体層に電気的に接続されるように前記データ線を形成し、

前記第１コンタクトホールを開孔する工程において、前記第１コンタクトホールを開孔すると同時に前記第１層

間絶縁膜に前記蓄積容量の一方の電極に通じる第４コンタクトホールを開孔し、前記第２導電層を形成する工程において、前記第４コンタクトホールを介して前記蓄積容量の一方の電極に電気的に接続されるように前記第２導電層を形成することを特徴とする請求項２３に記載の電気光学装置の製造方法。

【請求項２８】　基板に複数の走査線と、複数のデータ線と、前記各走査線と前記各データ線に接続された薄膜トランジスタと、前記薄膜トランジスタの接続された画素電極とを有する電気光学装置の製造方法において、

前記基板にソース領域、チャネル領域及びドレイン領域となる半導体層を形成する工程と、

前記半導体層上に絶縁薄膜を形成する工程と、

前記絶縁薄膜上に走査線及び蓄積容量の一方の電極を形成する工程と、

前記走査線及び蓄積容量の一方の電極上に第１層間絶縁膜を形成する工程と、

前記第１層間絶縁膜に前記半導体層に通じる第１コンタクトホールを開孔する工程と、

前記第１層間絶縁膜上にデータ線を形成すると同時に前記第１コンタクトホールを介して前記半導体層に電気的に接続されるように前記データ線と同一膜から中継導電層を形成する工程と、

前記データ線及び前記中継導電層上に第２層間絶縁膜を形成する工程と、

前記第２層間絶縁腺に前記中継導電層に通じる第２コンタクトホールを開孔する工程と、

前記第２層間絶縁膜上に前記第２コンタクトホールを介して前記中継導電層に電気的に接続されるように遮光性の第１導電層を形成すると同時に、前記第１導電層と同一膜からなる第２導電層を前記データ線に平面的に重なるように形成する工程と、

前記第１導電層及び前記第２導電層上に第３層間絶縁膜を形成する工程と、

前記第３層間絶縁膜に前記第１導電層に通じる第３コンタクトホールを開孔する工程と、

前記第３コンタクトホールを介して前記第１導電層に電気的に接続されるように画素電極を形成する工程とを含むことを特徴とする電気光学装置の製造方法。

【請求項２９】　前記第１層間絶縁膜を形成する工程の後に、前記第１層間絶縁膜に前記半導体層に通じる第４コンタクトホールを開孔する工程を更に含み、前記データ線を形成する工程において、前記第４コンタクトホールを介して前記半導体層に電気的に接続されるように前記データ線を形成し、

前記第２コンタクトホールを開孔する工程において、前記第２コンタクトホールを開孔すると同時に前記第１層間絶縁膜及び前記第２層間絶縁腺に前記蓄積容量の一方の電極に通じる第５コンタクトホールを開孔し、前記第２導電層を形成する工程において、前記第５コンタクト

ホールを介して前記蓄積容量の一方の電極に電気的に接続されるように前記第２導電層を形成することを特徴とする請求項２４に記載の電気光学装置の製造方法。

【請求項３０】　請求項１から請求項２５のいずれか一項に記載の電気光学装置を有することを特徴とする電子機器。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、電気光学装置及びその製造方法の技術分野に属し、特に画素電極と画素スイッチング用の薄膜トランジスタ（Thin Film Transistor以下適宜、ＴＦＴと称す）との間で電気的な導通を良好にとるための中継用の導電層を備える電気光学装置及びその製造方法並びに電子機器の技術分野に属する。

【０００２】

【従来の技術】従来この種の電気光学装置は、一対の基板間に液晶等の電気光学物質が扶持されてなり、一方の基板の一例であるＴＦＴアレイ基板には、マトリクス状に複数の画素電極が設けられ、他方の基板の一例である対向基板には、各画素における画素開口領域（即ち、各画素における電気光学物質部分を光が通過する領域）を規定するために、遮光膜が画素電極の間隙に対応して格子状に設けられるのが一般的である。この場合、各画素電極の周りで光漏れにより表示画像におけるコントラスト比が低下しないようにするため、平面的に見て各画素電極に格子状の遮光膜が若干重なるように構成されている。この際特に、対向基板側に設けられた遮光膜は、画素電極から電気光学物質等を介して比較的離れているために、斜めに入射する光や両基板の貼り合わせずれを考慮して、上述の如き画素電極と遮光膜とは、かなりのマージンで重ねる必要がある。これは、画素開口率（即ち、各画素における画素開口領域が占める率）を高める際の大きな障壁となる。

【０００３】そこで最近では、明るい画像表示を行うという一般的な要請の下、各画素における画素開口率を高めるために、対向基板側の遮光膜だけで画素開口領域を規定するのではなく、データ線をＡｌ（アルミニウム）等の遮光性材料から画素電極の縦方向の隙間を覆うように幅広に形成することにより、各画素開口領域を部分的に規定する技術も一般化している。この技術によれば、データ線によって画素開口領域を部分的に規定するようにしたので、画素開口率を高めることができる。

【０００４】他方、この種の電気光学装置においては、各画素電極と、例えば各画素に設けられたＴＦＴ等のスイッチング素子とは、相互に接続される必要があるが、両者間には、走査線、容量線、データ線等の配線及びこれらを相互に電気的に絶縁するための複数の層間絶縁膜を含む、例えば１０００ｎｍ（ナノメーター）程度又はそれ以上に厚い積層構造が存在するため、両者間を電気的に接続するためのコンタクトホールを開孔するのが困難となる。

【０００５】この種の電気光学装置における表示画像の高品位化という一般的な要請の下では、画素ピッチの微細化、画素開口率の向上、画素電極への画像信号の安定供給等が重要となる。

【０００６】しかしながら、前述したデータ線で画素開口領域を部分的に規定する技術によれば、データ線と画素電極とが層間絶縁膜を介して部分的に重なっているため、各画素に設けられたＴＦＴについて考えれば、上述したデータ線と画素電極との重なりに応じてソースとドレインとの間に寄生容量が生じてしまう。ここで一般に、データ線を介して画像信号が供給されるＴＦＴは、１フレーム期間に亘って画像信号に応じた一定電位を画素電極に保持させるようにスイッチング動作するが、この期間中にデータ線は、他行のＴＦＴに供給される画像信号の電位に頻繁に振れるので、上述のソースとドレインとの間の寄生容量により、ＴＦＴが異常動作して画素電極に保持させるべき電圧がリークしてしまう。この結果、画素電極への画像信号の供給が不安定となり、最終的には表示画像の劣化を招くという問題点がある。

【０００７】一方、この種の電気光学装置における装置構成の単純化や低コスト化という一般的な要請の下では、何らかの機能を付加或いは向上させる際にも、積層構造中の導電層や絶縁膜の数をむやみに増加させないこと、或いは一つの膜を複数機能を果たすために有効利用することが重要となる。

【０００８】本発明は上述の問題点に鑑みなされたものであり、比較的簡単な構成を有しており、画素開口率が高く、高品位の画像表示が可能な電気光学装置及びその製造方法を提供することを課題とする。

【０００９】

【課題を解決するための手段】本発明の電気光学装置は上記課題を解決するために、基板に、複数の走査線と、複数のデータ線と、前記各走査線及び前記各データ線の交差に対応して配置された薄膜トランジスタと画素電極と、前記薄膜トランジスタのソース及び、ドレイン領域を構成する半導体層と前記画素電極との間に介在し、前記半導体層と電気的に接続され且つ前記画素電極と電気的に接続された遮光性の第１導電層と、前記第１導電層と同一膜からなり、平面的に見て前記データ線に少なくとも部分的に重なっている第２導電層とを備える。

【００１０】本発明の電気光学装置の構成によれば、第１導電層は、半導体層と画素電極との間に介在しており、一方で半導体層と電気的に接続されており、他方で、画素電極と電気的に接続されている。従って、第１導電層は、画素電極と半導体層のドレイン領域とを電気的に接続するための中継用の導電層として機能し、例えば、両者間を一つのコンタクトホールを介して直接接続する場合の困難性を回避することが可能となる。

【００１１】また、第２導電層は平面的に見て前記デー

タ線に少なくとも部分的に重なっているため、データ線に加えて第２導電層により各画素の遮光を冗長させることが可能となる。

【００１２】本発明の電気光学装置の一の態様において、前記第２導電層は平面的に見て少なくとも部分的に前記画素電極に重なっている。

【００１３】この構成によれば、平面的に見て少なくとも部分的に隣接する画素電極の間に形成される第２導電層は、特に画素電極に重なっている。このため、この画素電極と部分的に重なった第２導電層部分により、各画素における画素開口領域を少なくとも部分的に規定できる。この際特に、第２導電層により画素開口領域が規定された個所では、平面的に見て画素電極と第２導電層との間に隙間はないため、そのような隙間を介しての光漏れは起こらない。この結果、最終的には、コントラスト比が高められる。同時に、第２導電層により画素開口領域が規定された個所では、従来のようにデータ線で画素開口領域を規定する必要はないため、データ線と画素電極とを重ねる必要もなくなる。この結果、データ線と画素電極とが層間絶縁膜を介して重なる構造により、各画素における薄膜トランジスタのソースとドレインとの間の寄生容量を発生させないで済む。このため、１フレーム等の所定周期内に他行の薄膜トランジスタに供給される画像信号の電位に頻繁に振れるデータ線の当該電位揺れに起因して、上述のソースとドレインとの間の寄生容量により薄膜トランジスタが異常動作して、画素電極に保持させるべき電圧がリークする事態を未然に防げる。即ち、画像信号に応じた一定電位を画素電極に保持させるように薄膜トランジスタはスイッチング動作し、データ線及び薄膜トランジスタを介して画素電極へ画像信号を安定供給でき、最終的には、フリッカやラインムラの低減により表示画像の高品位化が可能となる。

【００１４】更に、第１導電層に、薄膜トランジスタと画素電極とを中継する機能を持たせると共に、この第１導電層と同一膜からなる第２導電層に、画像信号の安定供給を可能ならしめつつ画素開口領域を規定する機能を持たせているので、全体として、積層構造及び製造プロセスの単純化並びに低コスト化を図れる。

【００１５】本発明の電気光学装置の他の態様において、前記第１導電層は、前記半導体層と第１コンタクトホールを介して電気的に接続され且つ前記画素電極と第２コンタクトホールを介して電気的に接続される。

【００１６】この構成によれば、画素電極から半導体層のドレイン領域まで一つのコンタクトホールを開孔する場合と比較して、コンタクトホールの径を小さくできる。即ち、一般にコンタクトホールを深く開孔する程、エッチング精度は落ちるため、薄い半導体層における突き抜けを防止するために、コンタクトホールの径を小さくできるドライエッチングを途中で停止して、最終的にウェットエッチングで半導体層まで開孔するように工程を組まねばならないので、指向性のないウェットエッチングによりコンタクトホールの径が広がらざるを得ないのである。これに対して本態様では、画素電極と半導体層間を２つの直列な第１及び第２コンタクトホールにより接続すればよいので、各コンタクトホールをドライエッチングにより開孔することが可能となるか、或いは少なくともウェットエッチングにより開孔する距離を短くすることが可能となる。この結果、各コンタクトホールの径を夫々小さくでき、第１又は第２コンタクトホールの上方に位置する画素電極部分における平坦化が促進される。

【００１７】本発明の電気光学装置の他の態様によれば、前記データ線は、前記半導体層と第３コンタクトホールを介して電気的に接続される。

【００１８】この構成によれば、データ線と半導体層のソース領域との電気的な接続が第３コンタクトホールを介して良好に得られる。

【００１９】本発明の電気光学装置の他の態様によれば、前記データ線は、平面的に見て前記画素電極に少なくとも部分的に重ならない。

【００２０】この構成によれば、データ線と画素電極とはできるだけ重ならないように形成することで、データ線と画素電極とを重ねるようにした場合と比較して、データ線と画素電極との間における寄生容量を確実に低減できる。従って、特に画素電極における電圧が安定してフリッカやラインムラを低減できる。

【００２１】更に、データ線と画素電極とが層間絶縁膜を介して重なった個所おいて発生する可能性が高い両者間の電気的ショート（短絡）等の欠陥の発生を抑えることができ、最終的には装置欠陥率の低下、製造時の歩留まり向上が図られる。

【００２２】本発明の電気光学装置の他の態様よれば、前記第２導電層は、定電位線に電気的に接続されている。

【００２３】この構成によれば、少なくとも部分に重なっている画素電極と第２導電層との間には、多少の寄生容量が付くが、第２導電層の電位が定電位に保たれている。このため、画素電極と第２導電層との間の寄生容量を介して、第２導電層の電位変動が画素電極の電位に及ぼす悪影響を低減でき、画素電極おける電圧がより安定してフリッカやラインムラを更に低減できる。

【００２４】本発明の電気光学装置の他の態様によれば、前記半導体層のうち少なくともチャネル領域の前記基板側に下地絶縁膜を介して形成された遮光膜を更に備える。

【００２５】この構成によれば、半導体層のうち少なくともチャネル領域の基板側に下地絶縁膜を介して形成された遮光膜により、ＴＦＴアレイ基板側からの光に対するチャネル領域の遮光を行うことができる。このため、当該電気光学装置の動作時において、投射光、裏面反射

光、反射光等の薄膜トランジスタへの光照射に起因して発生する、チャネル領域における光リークを低減し、薄膜トランジスタの特性変化や劣化を低減しつつ高品位の画像表示が可能となる。

【００２６】本発明の電気光学装置の他の態様によれば、前記第１導電層及び前記第２導電層は、高融点金属を含む。

【００２７】この構成によれば、凱導電層及び箭２導電層は、例えば、Ｔｉ（チタン）、Ｃｒ（クロム）、Ｗ（タングステン）、Ｔａ（タンタル）、Ｍｏ（モリブデン）及びＰｂ（鉛）のうちの少なくとも一つを含む、金属単体、合金、金属シリサイド等からなる。このため、製造プロセスにおいて第１導電層及び第２導電層形成後に行われる各種工程における高温処理で当該第１導電層及び第２導電層が変形したり破壊したりすることはない。

【００２８】本発明の電気光学装置の他の態様によれば、前記第２導電層と前記データ線とは、層間絶縁膜を介して少なくとも部分的に対向配置される。

【００２９】この構成によれば、保持すべき画像信号に応じて電位が変動する画素電極との間ではなく、電位がより安定した第２導電層との間で、データ線に容量が付加されるので、データ線の電位揺れを招かないようにしつつ適度に増加させることが可能ヒなる。特に画素ピッチを微細化して、これに伴いデータ線幅を微細化しても、第２導電層との間の容量を増加させることにより、データ線の容量不足を抑えることができ、当該データ線を介しての画像信号の画素電極への供給における書き込み能力不足を阻止できる。

【００３０】本発明の電気光学装置の他の態様によれば、前記画素電極に接続された蓄積容量を更に備える。

【００３１】この構成によれば、蓄積容量により、画素電極における画像信号の電圧保持時間を遥か長くすることができ、コントラスト比を非常に効率良く高められる。

【００３２】この態様では、前記第１導電層及び第２導電層は、前記走査線及び前記蓄積容量の一方の電極上に絶縁膜を介して設けられてもよい。

【００３３】この構成によれば、走査線及び蓄積容量の一方の電極上に絶縁膜を介して設けられた第１導電層により、画素電極と半導体層とを中継可能であり、走査線及び蓄積容量の一方の電極上に絶縁膜を介して設けられた第２導電層により、画素開口領域を規定可能であり、更に第２導電層と蓄積容量の一方の電極との間で容量を簡単に構成可能となる。

【００３４】この蓄積容量を更に備えた態様では、前記半導体層の一部からなる第１蓄積容量電極と前記蓄積容量の一方の電極である第２蓄積容量電極とが第１誘電体膜を介して対向配置され、前記第２蓄積容量電極と前記第１導電層の一部からなる第３蓄積容量電極とが前記絶縁膜である第２誘電体膜を介して対向配置されて前記蓄積容量が形成されてもよい。

【００３５】この構成によれば、半導体層の一部からなる第１蓄積容量電極と蓄積容量の一方の電極である第２蓄積容量電極とが第１誘電体膜を介して対向配置され、第１の蓄積容量が構成され、他方で、第２蓄積容量電極と第１導電層の一部からなる第３蓄積容量電極とが第２誘電体膜を介して対向配置されて第２の蓄積容量が構成される。そして、これら第１及び第２の蓄積容量から各画素電極に蓄積容量が形成されるので、非画素開口領域を有効利用して、しかも立体的な構造を利用して比較的大容量の蓄積容量を構築できる。

【００３６】この蓄積容量を更に備えた態様では、前記第２導電層は、前記第２蓄積容量電極に接続されてもよい。

【００３７】この構成によれば、少なくとも部分的に重なっている画素電極と第２導電層との間には、多少の寄生容量が付くが、第２導電層の電位が第２蓄積容量電極の電位に保たれる。

【００３８】このように第２導電層を第２蓄積容量電極に接続する場合には、前記第２導電層は、第４コンタクトホールを介して前記第２蓄積容量電極に接続されており、前記第４コンタクトホールは、前記第１コンタクトホールを開孔する工程と同一工程により開孔されてもよい。

【００３９】この構成によれば、比較的容易に第２導電層を第２蓄積容量電極に接続でき、しかも、第１コンタクトホールを開孔するのと同時に第４コンタクトホールを開孔するので、製造プロセスの単純化に役立つ。

【００４０】ここの第２蓄積容量電極は建設されて容量線としてもよい。

【００４１】この構成によれば、容量線は、定電位とされるか、或いは少なくとも大容量でありその電位変動は小さい。このため、画素電極と第２導電層との間の寄生容量を介して、第２導電層の電位変動が画素電極の電位に及ぼす悪影響を低減できる。

【００４２】この第２蓄積容量電極は遮光勝と接続されていても良い。

【００４３】この構成によれば、第２蓄積容量電極及び遮光膜の電位を同一にでき、第２蓄積容量電極及び遮光腺のいずれか一方を所定電位とする構成を採れば、他方の電位も所定電位とできる。この結果、第２蓄積容量電極や遮光膜における電位揺れによる悪影響を低減できる。また、遮光膜からなる配線と容量線とを相互に冗長配線として機能させることができる。

【００４４】この遮光膜は容量線を兼ね、前記第２蓄積容量電極は、前記基板上における平面形状が相隣接するデータ線間を前記走査線に沿って伸び、各画素電極毎に島状に構成されているとともに、前記遮光膜に接続されていてもよい。

【００４５】この構成によれば、第２蓄積容量電極を画素電極毎に島状に構成することができるため、画素開口率を向上させることができる。また、第２蓄積容量も配線とすれば、遮光膜とともに容量線の冗長配線にすることができる。

【００４６】さらに、前記遮光膜は、前記第４コンタクトホールとは異なる平面位置に開孔された第５コンタクトホールを介して前記容量線に電気的に接続されてもよい。

【００４７】この構成によれば、半導体層のうち少なくともチャネル領域の基板側に下地絶縁膜を介して形成された遮光膜により、基板側からの光に対するチャネル領域の遮光を行うことができる。しかも、遮光膜は、導電性であり、第５コンタクトホールを介して容量線に接続されているので、遮光膜を容量線の冗長配線として機能させることが可能となり、容量線の低抵抗化を図ることにより容量線の電位をより安定化させることにより、最終的には、表示画像の高品位化を図れる。また、第４コンタクトホールと第５コンタクトホールは、異なる平面位置に形成することにより、第４コンタクトホール及び第５コンタクトホールにおける接続不良を防止することができる。

【００４８】さらに、前記第２導電層と前記遮光膜とは前記第２蓄積容量電極を介して電気的に接続されてなり、前記第２導電層と前記遮光膜とは隣接する画素電極に接続されていてもよい。

【００４９】この構成によれば、第２導電層を容量線として利用することができる。また、第２蓄積容量電極を容量線とし、第２導電層と第２蓄積容量電極とを接続することにより、容量線を２重で形成することができ、冗長構造が実現できる。

【００５０】本発明の電気光学装置の他の態様によれば、前記第１導電層及び前記第２導電層は、前記データ線よりも下層に設けられている。

【００５１】この構成によれば、データ線よりも下層に設けられた第１導電層により、画素電極と半導体層とを中継可能であり、データ線よりも下層に設けられた第２導電層により、画素開口領域を規定可能であり、更に第１導電層と第２蓄積容量電極との間で容量を簡単に構成可能となる。

【００５２】本発明の電気光学装置の他の態様によれば、前記第２導電層は、平面的に見て島状に設けられており、画素開口領域のうち前記データ線に沿った領域を少なくとも部分的に規定する。

【００５３】この構成によれば、平面的に見て島状に設けられた第２導電層により、画素開口領域のうちデータ線に沿った領域を少なくとも部分的に規定可能である。例えば、データ線に沿った画素開口領域のうち、薄膜トランジスタのチャネル領域やデータ線と半導体層とを接続するコンタクトホールが開孔された領域を除く大部分の領域に第２導電層を形成することができ、この大部分の領域における画素開口領域を当該第２導電層で規定することが可能である。

【００５４】或いは、本発明の電気光学装置の他の態様によれば、前記第１導電層及び前記第２導電層は、前記データ線よりも前記基板から遠い層として、即ち上層に設けられていることを特徴とする。

【００５５】この構成によれば、データ線よりも基板から遠い層として設けられた第１導電層により、画素電極と半導体層とを中継可能であり、データ線よりも上層に設けられた第２導電層により、画素開口領域を規定可能である。この場合特に、第２導電層を、データ線上の全領域に層間絶縁膜を介して設けてもよいし、走査線上に層間絶縁膜を介して設けてもよい。また、第１導電層と画素電極とを接続するコンタクトホールの位置は、非開口領域内であれば任意の位置に設定できるので、設計自由度が増し有利である。

【００５６】この態様では、前記第２導電層は、平面的に見て前記第１導電層が存在する領域を除き前記格子状に設けられており、画素開口領域の前記データ線及び前記走査線に夫々沿った領域を規定するように構成してもよい。

【００５７】この構成によれば、第２導電層は、第１導電層が存在する領域を除き格子状に設けられているので、画素開口領域のデータ線及び走査線に夫々沿った領域を規定すること、即ち画素開口領域の輪郭の全てを規定することも可能である。尚、第１導電層と第２導電層との間隙については、例えば、対向基板側の遮光膜、薄膜トランジスタの下側の薄膜トランジスタ、データ線の延設部分等により、簡単に光漏れを防止できる。

【００５８】この第１導電層及び第２導電層が上層に設けられた態様では、前記半導体層と前記第１導電層とは前記データ線と同一膜からなる中継導電層を介して接続されていてもよい。

【００５９】この構成によれば、データ線よりも上層に設けられた第１導電層で、画素電極からデータ線と同一層からなる中継導電層までを電気的に接続し、この中継導電層により更に半導体層までを電気的に接続するようにしたので、二つの中継用の導電層である第１導電層と中継導電層により、画素電極から半導体層までを良好に中継可能となる。特にデータ線を構成するＡｌ膜と画素電極を構成するＩＴＯ（Indium Tin Oxide）膜との電気的な相性が悪い場合にも、これら両者と電気的に相性が良い材料（例えば、高融点金属）から第１導電層を形成すれば良い点で有利である。

【００６０】この第１導電層及び第２導電層が上層に設けられている態様では、前記画素電極に接続された蓄積容量を有し、前記データ線は前記蓄積容量の一方の電極と前記第２導電層との間に層間絶縁膜を介して扶持されてもよい。

【００６１】この構成によれば、保持すべき画像信号に応じて電位が変動する画素電極との間ではなく、電位がより安定した第２導電層及び蓄積容量の一方の電極との間で、データ線に容量を付加させることができるので、データ線の容量を電位揺れを招かないようにしつつ適度に増加させることが可能となる。特に画素ピッチを微細化して、これに伴いデータ線幅を微細化しても、第２導電層及び第２蓄積容量電極との間での容量を増加させることにより、データ線の容量不足を抑えることができ、当該データ線を介しての画像信号の画素電極への供給における書き込み能力不足を阻止できる。

【００６２】本発明の第１の電気光学装置の製造方法は上記課題を解決するために、基板に複数の走査線と、複数のデータ線と、前記各走査線と前記各データ線に接続された薄膜トランジスタと、前記薄膜トランジスタの接続された画素電極とを有する電気光学装置の製造方法において、前記基板にソース領域、チャネル領域及びドレイン領域となる半導体層を形成する工程と、前記半導体層上に絶縁薄膜を形成する工程と、前記絶縁薄膜上の所定領域に走査線及び蓄積容量の一方の電極を形成する工程と、前記走査線及び前記一方の電極上に第１層間絶縁膜を形成する工程と、前記絶縁薄膜及び前記第１層間絶縁膜に前記半導体層に通じる窮１コンタクトホールを開孔する工程と、前記第２絶縁膜上に、前記第１コンタクトホールを介して前記半導体層に電気的に接続されるように遮光性の第１導電層と、前記第１導電層と同一膜から第２導電層を形成する工程と、前記第１導電層及び前記第２導電層上に第２層間絶縁膜を形成する工程と、前記第２層間絶縁繰上に、データ線を形成する工程と、前記データ線上に第３層間絶縁膜を形成する工程と、前記第２層間絶縁膜及び前記第３層間絶縁膜に前記第１導電層に通じる第２コンタクトホールを開孔する工程と、前記第２コンタクトホールを介して前記第１導電層に電気的に接続されるように画素電極を形成する工程とを有し、前記第２導電層は、平面的に見て前記データ線に少なくとも部分的に重なるように形成されている。

【００６３】本発明の第１の電気光学装置の製造方法によれば、基板に、半導体層、絶縁薄膜、走査線及び蓄積容量の一方の電極並びに第１層間絶縁膜がこの順で積層形成される。次に、絶縁薄膜及び第１層間絶縁膜に半導体層に通じる第１コンタクトホールが開孔され、この第１コンタクトホールを介して半導体層に電気的に接続されるように遮光性の第１導電層が形成される。同時に、この第１導電層と同一膜から、平面的に見て画素電極が形成される領域の間隙内に少なくとも部分的に配置されるように第２導電層が形成される。続いて、第２層間絶縁膜、データ線、及び第３層間絶縁膜がこの順で積層形成される。次に、第１導電層に通じる第２コンタクトホールが開孔され、この第２コンタクトホールを介して第１導電層に電気的に接続されるように画素電離形成される。従って、上述したデータ線よりも基板に近い層として第１及び第２導電層を形成して二つのコンタクトホールを介して画素電極と半導体層とを第２導電層で中継する構成を有する本発明の電気光学装置を比較的容易に製造できる。特に、第１導電層と第２導電層とを同一膜から形成するので、製造プロセスの単純化並びに低コスト化を図れる。

【００６４】本発明の第１の電気光学装置の製造方法の一の態様では、前記第２層間絶縁膜を形成する工程の後に、前記第２層間絶縁膜に前記半導体層に通じる第３コンタクトホールを開孔する工程を更に含み、前記データ線を形成する工程において、前記第３コンタクトホールを介して前記半導体層に電気的に接続されるように前記データ線を形成し、前記第１コンタクトホールを開孔する工程において、前記第１コンタクトホールを開孔すると同時に前記第１層間絶縁膜に前記蓄積容量の一方の電極に通じる第４コンタクトホールを開孔し、前記第２導電層を形成する工程において、前記第４コンタクトホールを介して前記蓄積容量の一方の電極に電気的に接続されるように前記第２導電層を形成する。

【００６５】この構成によれば、第２層間絶縁膜の形成後、半導体層に通じる第３コンタクトホールが開孔され、この第３コンタクトホールを介して半導体層に電気的に接続されるようにデータ線が形成される。更に、第１コンタクトホールの開孔時に、同時に蓄積容量の一方の電極に通じる第４コンタクトホールが開孔され、この第４コンタクトホールを介して蓄積容量の一方の電極に電気的に接続されるように第２導電層が形成される。従って、上述したデータ線と半導体層とがコンタクトホールを介して電気的に接続されており第２導電層と蓄積容量の一方の電極とがコンタクトホールを介して電気的に接続された構成を有する本発明の電気光学装置を比較的容易に製造できる。特に、これら二つのコンタクトホールを同時に開孔するので、製造プロセスの単純化並びに低コスト化を図れる。

【００６６】本発明の第２の電気光学装置の製造方法は上記課題を解決するために、基板に複数の走査線と、複数のデータ線と、前記各走査線と前記各データ線に接続された薄膜トランジスタと、前記薄膜トランジスタの接続された画素電極とを有する電気光学装置の製造方法において、前記基板にソース領域、チャネル領域及びドレイン領域となる半導体層を形成する工程と、前記半導体層上に絶縁薄膜を形成する工程と、前記絶縁薄膜上に走査線及び蓄積容量の一方の電極を形成する工程と、前記走査線及び蓄積容量の一方の電極上に第１層間絶縁膜を形成する工程と、前記第１層間絶縁膜に前記半導体層に通じる第１コンタクトホールを開孔する工程と、前記第１層間絶縁膜上にデータ線を形成すると同時に前記第１コンタクトホールを介して前記半導体層に電気的に接続されるように前記データ線と同一膜から中継導電層を形

成する工程と、前記データ線及び前記中継導電層上に第２層間絶縁膜を形成する工程と、前記第２層間絶縁膜に前記中継導電層に通じる第２コンタクトホールを開孔する工程と、前記第２層間絶縁膜上に前記第２コンタクトホールを介して前記中継導電層に電気的に接続されるように遮光性の第１導電層を形成すると同時に、前記第１導電層と同一膜からなる第２導電層を前記データ線に平面的に重なるように形成する工程と、前記第１導電層及び前記第２導電層上に第３層間絶縁膜を形成する工程と、前記第３層間絶縁膜に前記第１導電層に通じる第３コンタクトホールを開孔する工程と、前記第３コンタクトホールを介して前記第１導電層に電気的に接続されるように画素電極を形成する工程とを含むことを特徴とする。

【００６７】本発明の第２の電気光学装置の製造方法によれば、基板に半導体層、絶縁薄膜、走査線及び蓄積容量の一方の電極並びに第１層間絶縁膜がこの順で積層形成される。次に、半導体層に通じるコンタクトホールが開孔され、データ線が形成されると同時に半導体層に電気的に接続されるようにデータ線と同一膜から中継導電層が形成される。次に、第２層間絶縁膜が形成された後、中継導電層に通じるコンタクトホールが開孔され、中継導電層に電気的に接続されるように遮光性の第１導電層が形成される。これと同時に、第１導電層と同一膜から第２導電層が形成される。続いて、第３層間絶縁膜が形成され、第１導電層に通じるコンタクトホールが開孔されて、第１導電層に電気的に接続されるように画素電極が形成される。従って、上述したデータ線と同一膜からなる導電層として中継導電層を形成すると共にデータ線よりも基板から遠い層、つまり上層として第１導電層を形成して三つのコンタクトホールを介して画素電極と半導体層とを中継導電層及び第１導電層で中継すると共に、画素開口領域を第２導電層で規定する構成を有する本発明の電気光学装置を比較的容易に製造できる。特に、第１導電層と第２導電層とを同一膜から形成するので、製造プロセスの単純化並びに低コスト化を図れる。

【００６８】本発明の第２の電気光学装置の製造方法の一の態様では、前記第１層間絶縁膜を形成する工程の後に、前記第１層間絶縁膜に前記半導体層に通じる第４コンタクトホールを開孔する工程を更に含み、前記データ線を形成する工程において、前記第４コンタクトホールを介して前記半導体層に電気的に接続されるように前記データ線を形成し、前記第２コンタクトホールを開孔する工程において、前記第２コンタクトホールを開孔すると同時に前記第１層間絶縁膜及び前記第２層間絶縁膜に前記蓄積容量の一方の電極に通じる第５コンタクトホールを開孔し、前記第２導電層を形成する工程において、前記第５コンタクトホールを介して前記蓄積容量の一方の電極に電気的に接続されるように前記第２導電層を形成する。

【００６９】この態様によれば、第１層間絶縁膜の形成後、半導体層に通じる第４コンタクトホールが開孔され、半導体層に電気的に接続されるようにデータ線が形成される。更に、第２層間絶縁膜にコンタクトホールを開孔する時に、同時に蓄積容量の一方の電極に通じるコンタクトホールが開孔され、蓄積容量の一方の電極に電気的に接続されるように第３導電層が形成される。従って、上述したデータ線と半導体層とがコンタクトホールを介して電気的に接続されており第２導電層と蓄積容量の一方の電極とがコンタクトホールを介して電気的に接続された構成を有する本発明の電気光学装置を比較的容易に製造できる。特に、これら二つのコンタクトホールを同時に開孔するので、製造プロセスの単純化並びに低コスト化を図れる。

【００７０】本発明のこのような作用及び他の利得は次に説明する実施の形態から明らかにする。

【００７１】

【発明の実施の形態】以下、本発明の実施形態を図面に基づいて説明する。

【００７２】（第１実施形態）本発明の第１実施形態における電気光学装置の構成について、図１から図４を参照して説明する。図１は、電気光学装置の画像表示領域を構成するマトリクス状に形成された複数の画素における各種素子、配線等の等価回路であり、図２は、データ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図であり、図３は、図２のＡ－Ａ’断面図であり、図４は、図２のＢ－Ｂ，断面図である。尚、図３及び図４においては、各層や各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならしめてある。

【００７３】図１において、本実施形態における電気光学装置の画像表示領域を構成するマトリクス状に形成された複数の画素は、走査線３ａとデータ線６ａの交差に対応して画素電極９ａを制御するためのＴＦＴ３０がマトリクス状に複数形成されており、画像信号が供給されるデータ線６ａが当該ＴＦＴ３０のソースに電気的に接続されている。データ線６ａに書き込む画像信号Ｓ１、Ｓ２、…、Ｓｎは、この順に線順次に供給しても構わないし、相隣接する複数のデータ線６ａ同士に対して、グループ毎に供給するようにしても良い。また、ＴＦＴ３０のゲートに走査線３ａが電気的に接続されており、所定のタイミングで、走査線３ａにパルス的に走査信号Ｇ１、Ｇ２、…、Ｇｍを、この順に線順次で印加するように構成されている。画素電極９ａは、ＴＦＴ３０のドレインに電気的に接続されており、スイッチング素子であるＴＦＴ３０を一定期間だけそのスイッチを閉じることにより、データ線６ａから供給される画像信号Ｓ１、Ｓ２、・・・、Ｓｎを所定のタイミングで書き込む。画素電極９ａを介して電気光学物質の一例として液晶に書き込まれた所定レベルの画像信号Ｓ１、Ｓ２、…、Ｓｎは、

対向基板（後述する）に形成された対向電極（後述する）との間で一定期間保持される。液晶は、印加される電圧レベルにより分子集合の配向や秩序が変化することにより、光を変調し、階調表示を可能にする。ノーマリーホワイトモードであれば、印加された電圧に応じて入射光がこの液晶部分を通過不可能とされ、ノーマリーブラックモードであれば、印加された電圧に応じて入射光がこの液晶部分を通過可能とされ、全体として電気光学装置からは画像信号に応じたコントラストを持つ光が出射する。ここで、保持された画像信号がリークするのを防くために、画素電極９ａと対向電極との間に形成される液晶容量と並列に蓄積容量７０を付加する。例えば、画素電極９ａの電圧は、ＴＦＴ３０のソースに画像信号が印加された時間よりも３桁も長い時間だけ蓄積容量７０により保持される。これにより、保持特性は更に改善され、コントラスト比の高い電気光学装置が実現できる。

【００７４】図２において、電気光学装置のＴＦＴアレイ基板上には、マトリクス状に複数の透明な画素電極９ａ（点線部９ａ’により輪郭が示されている）が設けられており、画素電極９ａの縦横の境界に各々沿ってデータ線６ａ、走査線３ａ及び容量線３ｂが設けられている。データ線６ａは、コンタクトホール５を介して例えはポリシリコン膜からなる半導体層１ａのうち後述の、ソース領域に電気的に接続されている。相隣接する画素電極９ａ間の間隙における走査線３ａに沿った領域及びデータ線６ａに沿った領域（図中右上がりの斜線で示した領域）には夫々、島状の第１導電層（以下、第１バリア層と称す）８０ａ及び第２導電層（以下、第２バリア層と称す）８０ｂが設けられている。本実施形態では特に、第１バリア層８０ａ及び第２バリア層８０ｂは同一の遮光性の導電膜から形成されている。画素電極９ａは、第１バリア層８０ａを中継して、コンタクトホール８ａ並びにコンタクトホール８ｂを介して半導体層１ａのうち後述のドレイン領域に電気的に接続されている。容量線３ｂは、第２バリア層８０ｂにコンタクトホール８ｃを介して電気的に接続されている。また、半導体層１ａのうち図中右下がりの斜線領域で示したチャネル領域１ａ’に対向するように走査線３ａが配置されており、走査線３ａはゲート電極として機能する。このように、走査線３ａとデータ線６ａとの交差する個所には夫々、チャネル領域１ａ’に走査線３ａがゲート電極として対向配置された画素スイッチング用ＴＦＴ３０が設けられている。

【００７５】容量線３ｂは、走査線３ａに沿ってほぼ直線状に伸びる本線部と、データ線６ａと交差する箇所からデータ線６ａに沿って突出した突出部とを有する。

【００７６】特に、第１バリア層８０ａは夫々、コンタクトホール８ａにより半導体層１ａのドレイン領域に電気的に接続されており、コンタクトホール８ｂにより画素電極９ａに電気的に接続されており、半導体層１ａのドレイン領域と画素電極９ａとの間におけるバッファとして機能している。この第１バリア層８０ａ、コンタクトホール８ａ並びにコンタクトホール８ｂについては後に詳述する。

【００７７】また、図中太線で示した領域には夫々、走査線３ａ、容量線３ｂ及びＴＦＴ３０の下側を通るように、第１遮光膜１１ａを設けても良い。第１遮光膜１１ａは夫々、走査線３ａに沿って縞状に形成するとともに、データ線６ａと交差する箇所が図中下方に幅広に形成し、この幅広の部分により画素スイッチング用ＴＦＴ３０のチャネル領域１ａ’をＴＦＴアレイ基板側から見て夫々覆う位置に設けるようにすると良い。

【００７８】次に図３の断面図に示すように、電気光学装置は、透明な一方の基板の一例を構成するＴＦＴアレイ基板１０と、これに対向配置される透明な他方の基板の一例を構成する対向基板２０とを備えている。ＴＦＴアレイ基板１０は、例えば石英基板、ガラス基板、シリコン基板からなり、対向基板２０は、，例えばガラス基板や石英基板からなる。ＴＦＴアレイ基板１０には、画素電極９ａが設けられており、その上側には、ラビング処理等の所定の配向処理が施された配向膜１６が設けられている。画素電極９ａは例えば、ＩＴＯ膜などの透明導電性薄膜からなる。また配向膜１６は例えば、ポリイミド薄膜などの有機薄膜からなる。

【００７９】他方、対向基板２０には、その全面に渡って対向電極２１が設けられており、その下側には、ラビング処理等の所定の配向処理が施された配向膜２２が設けられている。対向電極２１は例えば、ＩＴＯ膜などの透明導電性薄膜からなる。また配向膜２２は、ポリイミド薄膜などの有機薄膜からなる。

【００８０】ＴＦＴアレイ基板１０には、各画素電極９ａに隣接する位置に、各画素電極９ａをスイッチング制御する画素スイッチング用ＴＦＴ３０が設けられている。

【００８１】対向基板２０には、更に図３に示すように、各画素の非開口領域に、第２遮光膜２３が設けられている。このため、対向基板２０の側から入射光が画素スイッチング用ＴＦＴ３０の半導体層１ａのチヤネル領域１ａ’や低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃに侵入することはない。更に、第２遮光膜２３は、コントラストの向上、カラーフィルタを形成した場合における色材の混色防止などの機能を有する。

【００８２】このように構成され、画素電極９ａと対向電極２１とが対面するように配置されたＴＦＴアレイ基板１０と対向基板２０との間には、後述のシール材により囲まれた空間に電気光学物質の一例である液晶が封入され、液晶層５０が形成される。液晶層５０は、画素電極９ａからの電界が印加されていない状態で配向膜１６及び２２により所定の配向状態をとる。液晶層５０は、

例えば一種又は数種類のネマティック液晶を混合した液晶からなる。シール材は、ＴＦＴアレイ基板１０及び対向基板２０をそれらの周辺で貼り合わせるための、例えば光硬化性樹脂や熱硬化性樹脂からなる接着剤であり、両基板間の距離を所定値とするためのグラスファイバー或いはガラスビーズ等のギャップ材が混入されている。

【００８３】更に図３に示すように、画素スイッチング用ＴＦＴ３０に各々対向する位置においてＴＦＴアレイ基板１０と各画素スイッチング用ＴＦＴ３０との間には、第１遮光膜１１ａを設けるようにすると良い。第１遮光膜１１ａは、好ましくは不透明な高融点金属であるＴｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ及びＰｂのうちの少なくとも一つを含む、金属単体、合金、、金属シリサイド等から構成される。このような材料から構成すれば、ＴＦＴアレイ基板１０上の第１遮光膜１１ａの形成工程の後に行われる画素スイッチング用ＴＦＴ３０の形成工程における高温処理により、第１遮光膜１１ａが破壊されたり溶融しないようにできる。第１遮光膜１１ａが形成されているので、ＴＦＴアレイ基板１０の側からの反射光（戻り光）等が画素スイッチング用ＴＦＴ３０のチャネル領域１ａ’や低濃度ソース領域１ｂ、低濃度ドレイン領域１ｃに入射する事態を未然に防ぐことができ、これに起因した光による電流の発生により画素スイッチング用ＴＦＴ３０の特性が変化したり、劣化することはない。

【００８４】尚、縞状に形成された第１遮光膜１１ａは、例えば走査線３ａ下に延設されて、定電位線に電気的に接続されてもよい。このように構成すれば、第１遮光膜１１ａに対向配置される画素スイッチング用ＴＦＴ３０に対し第１遮光膜１１ａの電位変動が悪影響を及ぼすことはない。この場合、定電位線としては、当該電気光学装置を駆動するための周辺回路（例えば、走査線駆動回路、データ線駆動回路等）に供給される負電源、正電源等の定電位線、接地電源、対向電極２１に供給される定電位線等が挙げられる。尚、第１遮光膜１１ａはデータ線６ａ及び走査線３ａに沿って格子状で形成しても良いし、少なくとも画素スイッチング用ＴＦＴ３０のチャネル領域１ａ’や低濃度ソース領域１ｂ、低濃度ドレイン領域１ｃを覆うように島状に形成しても良い。

【００８５】更に、第１遮光膜１１ａと複数の画素スイッチング用ＴＦＴ３０との間には、下地絶縁膜１２が設けられている。下地絶縁膜１２は、画素スイッチング用ＴＦＴ３０を構成する半導体層１ａを第１遮光膜１１ａから電気的に絶縁するために設けられるものである。更に、下地絶縁膜１２は、ＴＦＴアレイ基板１０の全面に形成されることにより、画素スイッチング用ＴＦＴ３０のための下地膜としての機能をも有する。即ち、ＴＦＴアレイ基板１０の表面の研磨時における荒れや、洗浄後に残る汚れ等で画素スイッチング用ＴＦＴ３０の特性の劣化を防止する機能を有する。下地絶縁膜１２は、例えば、ＮＳＧ（ノンドープトシリケートガラス）、ＰＳＧ（リンシリケートガラス）、ＢＳＧ（ボロンシリケートガラス）、ＢＰＳＧ（ボロンリンシリケートガラス）などの高絶縁性ガラス又は、酸化シリコン膜、窒化シリコン膜等からなる。下地絶縁膜１２により、第１遮光膜１１ａが画素スイッチング用ＴＦＴ３０等を汚染する事態を未然に防ぐこともできる。

【００８６】本実施形態では、半導体層１ａを高濃度ドレイン領域１ｅから延設して第１蓄積容量電極１ｆとし、これに対向する容量線３ｂの一部を第２蓄積容量電極とし、ゲート絶縁膜を含んだ絶縁薄膜２を走査線３ａに対向する位置から延設してこれらの電極間に挟持された第１誘電体膜とすることにより、第１蓄積容量７０ａが構成されている。更に、この第２蓄積容量電極と対向する第１バリア層８０ａの一部を第３蓄積容量電極とし、これらの電極間に第１層間絶縁膜８１を設ける。第１層間絶縁膜８１は第２誘電体膜として機能し、第２蓄積容量７０ｂが形成されている。そして、これら第１蓄積容量７０ａ及び第２蓄積容遺７０ｂがコンタクトホール８ａを介して並列接続されて蓄積容量７０が構成されている。特に第１蓄積容量７０ａの第１誘電体膜としての絶縁薄膜２は、高温酸化によりポリシリコン膜上に形成されるＴＦＴ３０のゲート絶縁膜に他ならないので、薄く且つ高耐圧の絶縁膜とすることができ、第１蓄積容量７０ａは比較的小面積で大容量の蓄積容量として構成できる。また、第１層間絶縁膜８１も、絶縁薄膜２と同様に或いは絶縁薄膜２よりも薄く形成することができるので、第２蓄積容量７０ｂは比較的小面積で大容量の蓄積容量として構成できる。従って、これら第１蓄積容量７０ａ及び第２蓄積容量７０ｂから立体的に構成される蓄積容量７０は、データ線６ａ下の領域及び走査線３ａに沿って液晶のディスクリネーションが発生する領域（即ち、容量線３ｂが形成された領域）という画素開口領域を外れたスペースを有効に利用して、小面積で大容量の蓄積容量とされる。

【００８７】このように第２蓄積容量７０ｂを構成する第１層間絶縁膜８１は、酸化シリコン膜、窒化シリコン膜等でもよいし、多層膜から構成してもよい。一般にゲート絶縁膜等の絶縁薄膜２を形成するのに用いられる各種の公知技術（減圧ＣＶＤ法、プラズマＣＶＤ法、熱酸化法等）により、第１層間絶縁膜８１を形成可能である。第１層間絶縁膜８１を薄く形成することにより、コンタクトホール８ａの径を更に小さく出来るので、前述したコンタクトホール８ａにおける第１バリア層８０ａの窪みや凹凸が更に小さくて済み、その上方に位置する画素電極９ａにおける平坦化が更に促進される。

【００８８】図３において、画素スイッチング用ＴＦＴ３０は、ＬＤＤ（Lightly Doped Drain）構造を有しており、走査線３ａ、当該走査線３ａからの電界によりチャネルが形成される半導体層１ａのチャネル領域１

ａ’、走査線３ａと半導体層１ａとを絶縁するゲート絶縁膜を含む絶縁薄膜２、データ線６ａ、半導体層１ａの低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ、半導体層１ａの高濃度ソース領域１ｄ並びに高濃度ドレイン領域１ｅを備えている。高濃度ドレイン領域１ｅには、複数の画素電極９ａのうちの対応する一つが第１バリア層８０ａを中継して電気的に接続されている。低濃度ソース領域１ｂ及び高濃度ソース領域１ｄ並びに低濃度ドレイン領域１ｃ及び高濃度ドレイン領域１ｅは後述のように、半導体層１ａに対し、ｎ型又はｐ型のチャネルを形成するかに応じて所定濃度のｎ型用又はｐ型用の不純物をドープすることにより形成されている。ｎ型チャネルのＴＦＴは、動作速度が速いという利点があり、画素のスイッチング素子である画素スイッチング用ＴＦＴ３０として用いられることが多い。本実施形態では特にデータ線６ａは、Ａｌ等の低抵抗な金属膜や金属シリサイド等の合金膜などの遮光性且つ導電性の薄膜から構成されている。また、第１バリア層８０ａ及び第１層間絶縁膜８１の上には、高濃度ソース領域１ｄへ通じるコンタクトホール５及び第１バリア層８０ａへ通じるコンタクトホール８ｂが各々形成された第２層間絶縁膜４が形成されている。この高濃度ソース領域１ｄへのコンタクトホール５を介して、データ線６ａは高濃度ソース領域１ｄに電気的に接続されている。更に、データ線６ａ及び第２層間絶縁膜４の上には、第１バリア層８０ａへのコンタクトホール８ｂが形成された第３層間絶縁膜７が形成されている。このコンタクトホール８ｂを介して、画素電極９ａは第１バリア層８０ａに電気的に接続されており、更に第１バリア層８０ａを中継してコンタクトホール８ａを介して高濃度ドレイン領域１ｅに電気的に接続されている。前述の画素電極９ａは、このように構成された第３層間絶縁膜７の上面に設けられている。

【００８９】画素スイッチング用ＴＦＴ３０は、好ましくは上述のようにＬＤＤ構造を持つが、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃに不純物の打ち込みを行わないオフセット構造を持ってよいし、走査線３ａの一部からなるゲート電極をマスクとして高濃度で不純物を打ち込み、自己整合的に高濃度ソース及びドレイン領域を形成するセルフアライン型のＴＦＴであってもよい。

【００９０】また本実施形態では、画素スイッチング用ＴＦＴ３０のゲート電極を高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅ間に１個のみ配置したシングルゲート構造としたが、これらの間に２個以上のゲート電極を配置してもよい。この際、各々のゲート電極には同一の信号が印加されるようにする。このようにデュアルゲート或いはトリプルゲート以上でＴＦＴを構成すれば、チャネルとソース及びドレイン領域との接合部のリーク電流を防止でき、オフ時の電流を低減することができる。これらのゲート電極の少なくとも１個をＬＤＤ構造或いはオフセット構造にすれば、更にオフ電流を低減でき、安定したスイッチング素子を得ることができる。

【００９１】図２及び図３に示すように、本実施形態の電気光学装置では、高濃度ドレイン領域１ｅと画素電極９ａとをコンタクトホール８ａ及びコンタクトホール８ｂを介して第１バリア層８０ａを経由して電気的に接続するので、画素電極９ａからドレイン領域まで一つのコンタクトホールを開孔する場合と比較して、コンタクトホール８ａ及びコンタクトホール８ｂの径を夫々小さくできる。即ち、一つのコンタクトホールを開孔する場合には、コンタクトホールを深く開孔する程エッチング精度は落ちるため、例えば５０ｎｍ程度の非常に薄い半導体層１ａにおける突き抜けを防止するためには、コンタクトホールの径を小さくできるドライエッチングを途中で停止して、最終的にウエットエッチングで半導体層１ａまで開孔するように工程を組まねばならない。或いは、ドライエッチングによる突き抜け防止用のポリシリコン膜を別途設けたりする必要が生じてしまうのである。

【００９２】これに対して本実施形態では、画素電極９ａ及び高濃度ドレイン領域１ｅを２つの直列なコンタクトホール８ａ及びコンタクトホール８ｂにより接続すればよいので、これらコンタクトホール８ａ及びコンタクトホール８ｂを夫々、ドライエッチングにより開孔することが可能となるのである。或いは、少なくともウェットエッチングにより開孔する距離を短くすることが可能となるのである。但し、コンタクトホール８ａ及びコンタクトホール８ｂに、若干のテーパを付けるために、ドライエッチング後に敢えて比較的短時間のウエットエッチングを行うようにしてもよい。

【００９３】以上のように本実施形態によれば、コンタクトホール８ａ及びコンタクトホール８ｂの径を夫々小さくでき、コンタクトホール８ａにおける第１バリア層８０ａの表面に形成される窪みや凹凸も小さくて済むので、その上方に位置する画素電極９ａの部分における平坦化が、ある程度促進される。更に、第２コンタクトホール８ｂにおける画素電極９ａの表面に形成される窪みや凹凸も小さくて済むので、この画素電極９ａの部分における平坦化が、ある程度促進される。

【００９４】本実施形態では特に、第１バリア層８０ａは、導電性の遮光膜からなる。従って、第１バリア層８０ａにより、各画素開口領域を少なくとも部分的に規定することが可能となる。例えば、第１バリア層８０ａは、不透明な高融点金属であるＴｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ及びＰｂのうちの少なくとも一つを含む、金属単体、合金、金属シリサイド等から構成するようにする。これにより、コンタクトホール８ｂを介して第１バリア層８０ａ及び画素電極９ａ間で良好に電気的な接続がとれる。第１バリア層８０ａの膜厚は、例えば５０ｎｍ以

上５００ｎｍ以下程度とするのが好ましい。５０ｎｍ程度の厚みがあれば、製造プロセスにおける第２コンタクトホール８ｂの開孔時に突き抜ける可能性は低くなり、また５００ｎｍ程度であれば第１バリア層８０ａの存在に起因した画素電極９ａの表面の凹凸は問題とならないか或いは比較的容易に平坦化可能だからである。

【００９５】更に本実施形態では、各画素における画素関口領域のうち、データ線６ａに沿った領域の左右辺を、データ線６ａに沿って長手状に伸びる島状の第２バリア層８０ｂ及びコンタクトホール５周辺におけるデータ線６ａ部分から規定しており、各画素における画素開口領域のうち、走査線３ａ及び容量線３ｂに沿った領域の上辺及び下辺を第１バリア層８０ａ及び第１遮光膜１１ａにより夫々規定している。

【００９６】より具体的には図２及び図４に示すように、第２バリア層８０ｂは、平面的に見て部分的に画素電極９ａの間隙内に配置されており、画素電極９ａに部分的にも重なっている。このため、この画素電極９ａと第２バリア層８０ｂを一部重ねることにより、各画素における画素開口領域の左右辺の大部分を規定できる。この際特に、第２バリア層８０ｂにより画素開口領域が規定された個所では、平面的に見て画素電極９ａと第２バリア層８０ｂとの間に隙間はないため、そのような隙間を介しての光漏れは起こらない。この結果、最終的には、コントラスト比が高められる。同時に、第２バリア層８０ｂにより画素開口領域が規定された個所では、データ線６ａで画素開口領域を規定する必要はないため、この個所では、データ線６ａの幅は、第２バリア層８０ｂの幅よりも若干細められている。この結果、図４に示すように、データ線６ａと画素電極９ａとが第３層間絶縁膜７を介して重ならないようにすることにより、各画素におけるＴＦＴ３０のソースとドレインとの間の寄生容量を発生させないで済む。このため、１フレーム等の所定周期内に他行のＴＦＴ３０に供給される画像信号の電位に頻繁に振れるデータ線６ａの当該電位揺れに起因して、上述のソースとドレインとの間の寄生容量によりＴＦＴ３０が異常動作して、画素電極９ａに保持させるべき電圧がリークする事態を未然に防げる。これらの結果、表示画像におけるフリッカやラインムラを低減できる。但し、第２バリア層８０ｂが存在しないコンタクトホール５周辺の比較的小さい領域では、データ線６ａの幅を若干太めるようにして、データ線６ａにより画素開口領域を規定してもよい。

【００９７】また、以上のように画素開口領域を規定するように構成すれば、対向基板２０に第２遮光膜２３を形成しなくて済むため、対向基板のコストを削減することが可能である。更に、対向基板２０とＴＦＴアレイ基板１０とのアライメントずれによる画素開口率の低下やばらつきを防ぐことができる。また、対向基板２０に第２遮光膜２３を設ける場合は、ＴＦＴアレイ基板１０とのアライメントずれにより画素開口率を低減しないように小さめに形成しても上述のようにデータ線６ａ、第１バリア層８０ａ及び第２バリア層８０ｂ並びに第１遮光膜１１ａというＴＦＴアレイ基板１０側に形成された遮光性の膜により画素関口部を規定するため、精度よく画素開口部を規定することができ、対向基板２０上の第２遮光膜２３こより画素開口部を決める場合に比べて画素開口率を向上させることができる。

【００９８】更に図２及び図４に示したようにデータ線６ａの幅を若干狭めて画素電極９ａの縁部分と重ならない構成とすることにより、データ線６ａと画素電極９ａとが第３層間絶縁膜７を介して重なった個所において発生する可能性が高い両者間の電気的ショート（短絡）等の欠陥の発生を抑えることができ、最終的には装置欠陥率の低下、製造時の歩留まり向上が滑られる。

【００９９】第２バリア層８０ｂは、好ましくは、容量線３ｂや他の定電位線に電気的に接続される。即ち、第２バリア層８０ｂの縁部分と画素電極９ａの縁部分が重なるために、両者間には多少の寄生容量が付加されるが、第２バリア層８０ｂの電位が一定電位に保たれていれば、第２バリア層８０ｂの電位変動が画素電極９ａの電位に及ぼす悪影響を低減できる。尚、第２バリア層８０ｂと容量線３ｂとを電気的に接続するためのコンタクトホール８ｃは、本実施形態では、コンタクトホール８ａを開孔する工程と同一工程により開孔可能であり、製造プロセスの複雑化を招かない。尚、この場合、第２バリア層８０ｂは、各画素毎に、コンタクトホール８ｃを介して容量線３ｂに電気的に接続される。

【０１００】更にまた上述の如く第２バリア層８０ｂとデータ線６ａとが第２層間絶縁膜４を介して対向配置された構成においては、データ線６ａには、電位がより安定した第２バリア層８０ｂとの間で容量が付加される。このため、データ線６ａの容量を電位揺れを招かないような適度な大きさに設定できる。特に画素ピッチを微細化して、これに伴いデータ線６ａの幅を微細化しても、第２バリア層８０ｂとの間の容量を増加させることにより、データ線６ａの容量不足を抑えることができる。これにより、データ線６ａを介しての画像信号の画素電極９ａへの供給における書き込み能力不足を阻止できる。言い換えれば、特に画素ピッチを微細化する際に有利な、データ線６ａがノイズに対して強くなる構造が比較的容易に得られる。

【０１０１】尚、本実施形態の各コンタクトホール（８ａ、８ｂ、８ｃ及び５）の平面形状は、円形や四角形或いはその他の多角形状等でもよいが、円形は特にコンタクトホールの周囲の層間絶縁膜等におけるクラック防止に役立つ。そして、良好に電気的な接続を得るために、ドライエッチング後にウエットエッチングを行って、これらのコンタクトホールに夫々若干のテーパをつけることが好ましい。

【０１０２】以上説明したように第１実施形態の電気光学装置によれば、第１バリア層８０ａに、ＴＦＴ３０と画素電極９ａとを中継する機能を持たせると共に、この第１バリア層８０ａと同一膜からなる第２バリア層８０ｂに、画像信号の安定供給を可能ならしめつつ画素開口領域を規定する機能を持たせているので、全体として、積層構造及び製造プロセスの単純化並びに低コスト化を図れる。

【０１０３】（第１実施形態における電気光学装置の製造プロセス）次に、以上のような構成を持つ実施形態における電気光学装置を構成するＴＦＴアレイ基板の製造プロセスについて、図５から図８を参照して説明する。尚、図５から図８は各工程におけるＴＦＴアレイ基板側の各層を、図３と同様に図２のＡ－Ａ’断面に対応させて示す工程図である。

【０１０４】先ず図５の工程（１）に示すように、石英基板、ハードガラス基板、シリコン基板等のＴＦＴアレイ基板１０を用意する。ここで、好ましくはＮ２（窒素）等の不活性ガス雰囲気且つ約９００～１３００℃の高温で熱処理し、後に実施される高温プロセスにおけるＴＦＴアレイ基板１０に生じる歪みが少なくなるように前処理しておく。即ち、製造プロセスにおける最高温で高温処理される温度に合わせて、事前にＴＦＴアレイ基板１０を同じ温度かそれ以上の温度で熱処理しておく。そして、このように処理されたＴＦＴアレイ基板１０の全面に、Ｔｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ及びＰｂ等の金属や金属シリサイド等の金属合金膜を、スパッタリング等により、１００～５００ｎｍ程度の膜厚、好ましくは約２００ｎｍの膜厚の遮光膜１１を形成する。尚、遮光膜１１上には、表面反射を緩和するためにポリシリコン膜等の反射防止膜を形成しても良い。

【０１０５】次に工程（２）に示すように、該形成された遮光膜１１上にフォトリソグラフイにより第１遮光膜１１ａのパターンに対応するレジストマスクを形成し、該レジストマスクを介して遮光膜１１に対しエッチングを行うことにより、第１遮光膜１１ａを形成する。

【０１０６】次に工程（３）に示すように、第１遮光膜１１ａの上に、例えば、常圧又は減圧ＣＶＤ法等によりＴＥＯＳ（テトラ・エチル・オルソ・シリケート）ガス、ＴＥＢ（テトラ・エチル・ボートレート）ガス、ＴＭＯＰ（テトラ・メチル・オキシ・フオスレート）ガス等を用いて、ＮＳＧ（ノンシリケートガラス）、ＰＳＧ（リンシリケートガラス）、ＢＳＧ（ボロンシリケートガラス）、ＢＰＳＧ（ポロンリンシリケートガラス）などのシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等からなる下地絶縁膜１２を形成する。この下地絶縁膜１２の膜厚は、例えば、約５００～２０００ｎｍとする。

【０１０７】次に工程（４）に示すように、下地絶縁膜１２の上に、約４５０～５５０℃、好ましくは約５００℃の比較的低温環境中で、流量約４００～６００ｃｃ／ｍｉｎのモノシランガス、ジシランガス等を用いた減圧ＣＶＤ（例えば、圧力約２０～４０ＰａのＣＶＤ）により、アモルファスシリコン膜を形成する。その後、窒素雰囲気中で、約６００～７００℃にて約１～１０時間、好ましくは、４～６時間の熱処理を施すことにより、ポリシリコン膜１を約５０～２００ｎｍの厚さ、好ましくは約１００ｎｍの厚さとなるまで固相成長させる。固相成長させる方法としては、ＲＴＡ（Rapid Thermal Anneal）を使った熱処理でも良いし、エキシマレーザー等を用いたレーザー熱処理でも良い。

【０１０８】この際、図３に示した画素スイッチング用ＴＦＴ３０として、ｎチャネル型の画素スイッチング用ＴＦＴ３０を作成する場合には、当該チャネル領域にＳｂ（アンチモン）、Ａｓ（砒素）、Ｐ（リン）などのＶ族元素の不純物を僅かにイオン注入等によりドープしても良い。また、画素スイッチング用ＴＦＴ３０をｐチャネル型とする場合には、Ｂ（ボロン）、Ｇａ（ガリウム）、Ｉｎ（インジウム）などのIII族元素の不純物を僅かにイオン注入等によりドープしても良い。尚、アモルファスシリコン膜を経ないで、減圧ＣＶＤ法等によりポリシリコン膜１を直接形成しても良い。或いは、減圧ＣＶＤ法等により堆積したポリシリコン膜にシリコンイオンを打ち込んで一旦非晶質化し、その後熱処理等により再結晶化させてポリシリコン膜１を形成しても良い。

【０１０９】次に工程（５）に示すように、フォトリソグラフィ工程、エッチング工程等により、第1蓄積容量電極１ｆを含む所定パターンを有する半導体層１ａを形成する。

【０１１０】次に工程（６）に示すように、画素スイッチング用ＴＦＴ３０を構成する半導体層１ａを約９００～１３００℃の温度、好ましくは約１０００℃の温度により熱酸化することにより、約３０ｎｍの比較的薄い厚さの熱酸化シリコン膜２ａを形成し、更に工程（７）に示すように、減圧ＣＶＤ法等により高温酸化シリコン膜（ＨＴＯ膜）や窒化シリコン膜からなる絶縁膜２ｂを約５０ｎｍの比較的薄い厚さに堆積し、熱酸化シリコン膜２ａ及び絶縁膜２ｂを含む多層構造を持つ画素スイッチング用ＴＦＴ３０のゲート絶縁膜と共に蓄積容量形成用の第１誘電体膜を含む絶縁薄膜２を形成する。この結果、半導体層１ａの厚さは、約３０～１５０ｎｍの厚さ、好ましくは約３５～５０ｎｍの厚さとなり、絶縁薄膜２の厚さは、約２０～１５０ｎｍの厚さ、好ましくは約３０～１００ｎｍの厚さとなる。このように高温熱酸化時間を短くすることにより、特に８インチ程度の大型基板を使用する場合に熱によるそりを防止することができる。但し、ポリシリコン膜１を熱酸化することのみにより、単一層構造を持つ絶縁薄膜２を形成してもよい。

【０１１１】次に工程（８）に示すように、フォトリソグラフィ工程、エッチング工程等によりレジスト層５０

０を第１蓄積容量電極１ｆとなる部分を除く半導体層１ａ上に形成した後、例えばＰイオンをドーズ量約３×１０^{12}／ｃｍ^{2}でドープして、第１蓄積容量電極１ｆを低抵抗化する。

【０１１２】次に工程（９）に示すように、レジスト層５００を除去した後、減圧ＣＶＤ法等によりポリシリコン膜３を堆積し、更にＰを熱拡散し、ポリシリコン膜３を導電化する。又は、Ｐイオンをポリシリコン膜３の成膜と同時に導入した低抵抗なポリシリコン膜を用いてもよい。ポリシリコン膜３の膜厚は、約１００～５００ｎｍの厚さ、好ましくは約３００ｎｍに堆積する。

【０１１３】次に図６の工程（１０）に示すように、レジストマスクを用いたフォトリソグラフィ工程、エッチング工程等により、所定パターンの走査線３ａと共に容量線３ｂを形成する。走査線３ａ及び容量線３ｂは、高融点金属や金属シリサイド等の金属合金膜で形成しても良いし、ポリシリコン膜等と組み合わせた多層配線としても良い。

【０１１４】次に工程（１１）に示すように、図３に示した画素スイッチング用ＴＦＴ３０をＬＤＤ構造を持つｎチャネル型のＴＦＴとする場合、半導体層１ａに、先ず低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃを形成するために、走査線３ａの一部からなるゲート電極をマスクとして、ＰなどのＶ族元素の不純物を低濃度で、例えば、Ｐイオンを１～３×１０^{13}／ｃｍ^{2}のドーズ量にてドープする。これにより走査線３ａ下の半導体層１ａはチャネル領域１ａ’となる。この不純物のドープにより容量線３ｂ及び走査線３ａも低抵抗化される。

【０１１５】次に工程（１２）に示すように、画素スイッチング用ＴＦＴ３０を構成する高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅを形成するために、走査線３ａよりも幅の広いマスクでレジスト層６００を走査線３ａ上に形成した後、同じくＰなどのＶ族元素の不純物を高濃度で、例えば、Ｐイオンを１～３×１０^{15}／ｃｍ^{2}のドーズ量にてドープする。また、画素スイッチング用ＴＦＴ３０をｐチャネル型とする場合、半導体層１ａに、低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃ並びに高濃度ソース領域１ｄ及び高濃度ドレイン領域１ｅを形成するために、ＢなどのIII族元素の不純物を用いてドープする。尚、例えば、低濃度のドープを行わずに、オフセット構造のＴＦＴとしてもよく、走査線３ａをマスクとして、Ｐイオン、Ｂイオン等を用いたイオン注入技術によりセルフアライン型のＴＦＴとしてもよい。この不純物のドープにより容量線３ｂ及び走査線３ａも更に低抵抗化される。

【０１１６】尚、これらのＴＦＴ３０の素子形成工程と並行して、ｎチャネル型ＴＦＴ及びｐチャネル型ＴＦＴから構成される相補型構造を持つデータ線駆動回路、走査線駆動回路等の周辺回路をＴＦＴアレイ基板１０上の周辺部に形成してもよい。このように、本実施形態において画素スイッチング用ＴＦＴ３０を構成する半導体層１ａをポリシリコン膜で形成すれば、画素スイッチング用ＴＦＴ３０の形成時にほぼ同一工程で、周辺回路を形成することができ、製造上有利である。

【０１１７】次に工程（１３）に示すように、レジスト層６００を除去した後、容量線３ｂ及び走査線３ａ並びに絶縁薄膜２上に、減圧ＣＶＤ法、プラズマＣＶＤ法等により高温酸化シリコン膜（ＨＴＯ膜）や窒化シリコン膜からなる第１層間絶縁膜８１を約２００ｎｍ以下の比較的薄い厚さに堆積する。但し、前述のように、第１層間絶縁膜８１は、多層膜から構成してもよいし、一般にＴＦＴのゲート絶縁膜を形成するのに用いられる各種の公知技術により、第１層間絶縁膜８１を形成可能である。

【０１１８】次に工程（１４）に示すように、第１バリア層８０ａと高濃度ドレイン領域１ｅとを電気的に接続するためのコンタクトホール８ａ並びに第２バリア層８０ｂと容量線３ｂとを電気的に接続するためのコンタクトホール８ｃを、反応性イオンエッチング、反応性イオンビームエッチング等のドライエッチングにより形成する。このようなドライエッチングは、指向性が高いため、小さな径のコンタクトホール８ａ及びコンタクトホール８ｃを開孔可能である。或いは、コンタクトホール８ａが半導体層１ａを突き抜けるのを防止するのに有利なウェットエッチングを併用してもよい。このウェットエッチングは、コンタクトホール８ａに対し、より良好に電気的な接続をとるためのテーパを付与する観点からも有効である。また特に、コンタクトホール８ａ及びコンタクトホール８ｃは上述にように同時に開孔可能であり製造上有利である。

【０１１９】次に工程（１５）に示すように、第１層間絶縁膜８１並びにコンタクトホール８ａを介して覗く高濃度ドレイン領域１ｅ及びコンタクトホール８ｃを介して覗く容量線３ｂの全面に、Ｔｉ、Ｃｒ、Ｗ、Ｔａ、Ｍｏ及びＰｂ等の金属や金属シリサイド等の金属合金膜をスパッタリング等により堆積して、５０～５００ｎｍ程度の膜厚の導電膜８０を形成する。５０ｎｍ程度の厚みがあれば、後にコンタクトホール８ｂを開孔する時に突き抜ける可能性は殆どない。尚、この導電膜８０上には、表面反射を緩和するためにポリシリコン膜等の反射防止膜を形成しても良い。尚、導電膜８０は金属や金属シリサイド等の金属合金膜あるいは、ポリシリコン膜を積層した多層膜であってもよい。

【０１２０】次に図７の工程（１６）に示すように、該形成された導電膜８０上にフォトリソグラフィ工程及びエッチング工程等を行うことにより、第１バリア層８０ａ及び第２バリア層８０ｂを形成する。ここで第２バリア層８０ｂについては特に図４に示したように、その一部分が後で形成される画素電極９ａと若干重なるように形成すると良い。

【０１２１】次に工程（１７）に示すように、第１層間絶縁膜８１並びに第１バリア層８０ａ及び第２バリア層８０ｂを覆うように、例えば、常圧又は減圧ＣＶＤ法やＴＥＯＳガス等を用いて、ＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧなどのシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等からなる第２層間絶縁膜４を形成する。第２層間絶縁膜４の膜厚は、約５００～１５００ｎｍが好ましい。第２層間絶縁膜４の膜厚が５００ｎｍ以上あれば、データ線６ａ及び走査線３ａ間における寄生容量は余り又は殆ど問題とならない。

【０１２２】次に工程（１８）の段階で、半導体層１ａを活性化するために約１００００°Ｃの熱処理を２０分程度行った後、データ線６ａと半導体層１ａの高濃度ドレイン領域１ｅを電気的に接続するためのコンタクトホール５を絶縁薄膜２、第１層間絶縁膜８１及び第２層間絶縁膜４に開孔する。また、走査線３ａや容量線３ｂを基板周辺領域において図示しない配線と接続するためのコンタクトホールも、コンタクトホール５と同一の工程により開孔することができる。

【０１２３】次に、工程（１９）に示すように、第２層間絶縁膜４の上に、スパッタリング等により、遮光性のＡｌ等の低抵抗金属や金属シリサイド等を金属膜６として、約１００～５００ｎｍの厚さ、好ましくは約３００ｎｍに堆積する。

【０１２４】次に工程（２０）に示すように、フォトリソグラフイ工程及びエッチング工程等により、データ線６ａを形成する。ここでデータ線６ａについては特に図４に示したように、後で形成される画素電極９ａに重ならないように且つ第２バリア層８０ｂに重なるように形成する。

【０１２５】次に図８の工程（２１）に示すように、データ線６ａ上を覆うように、例えば、常圧又は減圧ＣＶＤ法やＴＥＯＳガス等を用いて、ＮＳＧ、ＰＳＧ、ＢＳＧ、ＢＰＳＧなどのシリケートガラス膜、窒化シリコン膜や酸化シリコン膜等からなる第３層間絶縁膜７を形成する。第３層間絶縁膜７の膜厚は、約５００～１５００ｎｍが好ましい。

【０１２６】次に工程（２２）に示すように、画素電極９ａと第１バリア層８０ａとを電気的に接続するためのコンタクトホール８ｂを、反応性イオンエッチング、反応性イオンビームエッチング等のドライエッチングにより形成する。テーパ状にするためにウェットエッチングを追加しても良い。

【０１２７】次に工程（２３）に示すように、第３層間絶縁膜７の上に、スパッタリング等により、ＩＴＯ膜等の透明導電性薄膜９を、約５０～２００ｎｍの厚さに堆積し、更に工程（２４）に示すように、フォトリソグラフィ工程及びエッチング工程等により、画素電極９ａを形成する。尚、当該電気光学装置を反射型として用いる場合には、Ａｌ等の反射率の高い不透明な材料から画素電極９ａを形成してもよい。

【０１２８】以上説明したように本実施形態における製造プロセスによれば、比較的少ない工程数で且つ比較的簡単な各工程を用いて上述した第１実施形態の電気光学装置を製造できる。

【０１２９】（第２実施形態）本発明の第２実施形態における電気光学装置の構成について、図９から図１１を参照して説明する。図９は、第２実施形態におけるデータ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図であり、図１０は、そのＡ－Ａ’断面図であり、図１１は、そのＢ－Ｂ’断面図である。また、図１０及び図１１においては、各層や各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならしめてある。尚、図９から図１１に示した第２実施形態において図２から図４に示した第１実施形態と同様の構成要素については、同様の参照符号を付し、その説明は省略する。

【０１３０】図９から図１１において、第２実施形態では、半導体層１ａの高濃度ドレイン領域１ｅにコンタクトホール８８ａを介して電気的に接続されておりデータ線６ａと同一層から構成された中継導電層６ｂと、画素電極９ａにコンタクトホール８８ｃを介して電気的に接続された遮光性の導電層からなる第１バリア層９０ａとを備えている。そして、中継導電層６ｂと第１バリア層９０ａとは、データ線６ａ及び中継導電層６ｂ上に形成された第２層間絶縁膜４を介して対向配置されており、この第２層間絶縁膜４に開孔されたコンタクトホール８８ｂを介して相互に電気的に接続されている。他方、第２実施形態では、第１バリア層９０ａと同一の遮光性の導電層からなる第２バリア層９０ｂが設けられており、第２バリア層９０ｂと容量線３ｂとは、コンタクトホール８８ｄを介して電気的に接続されている。これにより、第２バリア層９０ｂを蓄積容量電極とし、かつ隣接する画素群と接続することにより、容量線として代用できる。この場合、容量線３ｂを蓄積容量電極として、各画素毎に島状に形成しても良い。これにより、画素開口率を大きくすることができる。また、第２バリア層９０ｂと容量線３ｂを電気的に接続することにより、容量線を２重で形成することができ、冗長構造が実現できる。図９に示すように、第２バリア層９０ｂは、平面的に見て第１バリア層９０ａが存在する領域の周囲を除き画素電極９ａの間隙を覆う格子状に設けられており、画素開口領域のうちデータ線６ａ及び走査線３ａに夫々沿った左右辺及び上下辺を規定する。この場合にも第１実施形態の場合と同じく、第２バリア層９０ｂの縁部分は、画素電極９ａの縁部分に若干重ねられる。尚、第１バリア層９０ａと第２バリア層９０ｂとの間隙については、中継導電層６ｂや対向基板側の第２遮光膜２３で覆うことにより、簡単に光漏れを防止できる。その他の構成については第１実施形態の場合と同様である。

【０１３１】このように第２実施形態では、二つの中継用の導電層である中継導電層６ｂ及び第１バリア層９０ａにより、画素電極９ａから半導体層１ａまでを良好に中継可能となる。特に画素電極９ａがＩＴＯ膜からなりデータ線６ａがＡｌ膜からなる場合には、両者との間で良好に電気的な接続が得られるＴｉ、Ｃｒ、Ｗ等の高融点金属等から構成するのが好ましい。

【０１３２】また、図１１に示すように、データ線６ａが容量線３ｂとバリア層９０ｂとの間に誘電体膜である第１層間絶縁膜８１及び第２層間絶縁膜４を介して挟持された構成においては、データ線６ａには、電位がより安定した容量線３ｂ及び第２バリア層９０ｂとの間で容量が付加される。このため、データ線６ａの容量を電位揺れを招かないような適度な大きさに設定でき、データ線６ａを介しての画像信号の画素電極９ａへの供給における書き込み能力不足を阻止できる。

【０１３３】このようなＡｌ膜と同一膜からなる中継導電層６ｂは、例えば、第１実施形態の製造プロセスにおける工程（１８）において、高濃度ドレイン領域１ｅに至るコンタクトホール８８ａを開孔し、工程（２０）において、このコンタクトホール８８ａの部分を含めて高濃度ドレイン領域１ｅの上方に中継導電層６ｂを形成するのに、工程（１９）で形成したＡｌ膜に対してフォトリソグラフィ工程及びエッチング工程等を施せばよい。更に第２層間絶縁膜４並びに第１バリア層９０ａ及び第２バリア層９０ｂについては、データ線６ａ及び中継導電層６ｂ上に、第１実施形態における工程（１３）から工程（１６）と同様のプロセスにより形成すればよい。

【０１３４】（第３実施形態）本発明の第３実施形態における電気光学装置の構成について、図１２を参照して説明する。図１２は、第３実施形態におけるデータ線、走査線、画素電極等が形成された断面図に対応する断面図である。また、図１２においては、各層や各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならしめてある。尚、図１２に示した第３実施形態において図１０に示した第２実施形態と同様の構成要素については、同様の参照符号を付し、その説明は省略する。

【０１３５】図１２において、第３実施形態では、第２実施形態とは異なり、中継導電層６ｂを用いることなく、第１バリア層９０ａ’で直接高濃度ドレイン領域１ｅとの間で電気的な接続がとれるように構成されている。その他の構成については、第２実施形態の場合と同様である。

【０１３６】従って、第３実施形態によれば、画素電極９ａを構成するＩＴＯ膜と電気的に相性の良い高融点金属膜から構成される第１バリア層９０ａ’により、画素電極９ａと高濃度ドレイン領域１ｅとを電気的に中継接続することができる。

【０１３７】（第４実施形態）本発明の第４実施形態における電気光学装置の構成について、図１３から図１５を参照して説明する。図１３は、第４実施形態におけるデータ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図であり、図１４は、そのＡ－Ａ’断面図であり、図１５は、そのＢ－Ｂ’断面図である。また、図１４及び図１５においては、各層や各部材を図面上で認識可能な程度の大きさとするため、各層や各部材毎に縮尺を異ならしめてある。尚、図１３から図１５に示した第４実施形態において図２から図４に示した第１実施形態と同様の構成要素については、同様の参照符号を付し、その説明は省略する。

【０１３８】図１３から図１５において、第４実施形態では、第１実施形態とは異なり、第１遮光膜１１ａ’が相隣接する画素電極９ａの間隙を縫って格子状に形成されており、容量線３ｂがコンタクトホール１５を介して各画素毎に第１遮光腺１１ａ’に電気的に接続されている。第１遮光膜１１ａ’を容量線３ｂの冗長配線として機能させることが可能であり、容量線３ｂの低抵抗化を図ることにより蓄積容量７０の電位を安定化させることができる。また、この構成では、第１遮光膜１１ａ’を容量線として代用することで、容量線３ｂを各画素毎に島状の蓄積容量電極として構成しても良い。これにより、画素開口率を大きくすることができる。また、第２実施形態と組み合わせることで、容量線３ｂを第１遮光膜１１ａ’と第２バリア層９０ｂと電気的に接続することにより、蓄積容量を形成するための容量線を３重配線にしても良い。容量線３ｂを蓄積容量電極として島状に各画素毎に形成する場合は、第１遮光膜１１ａ’と第２バリア層９０ｂは蓄積容量電極を介して電気的に接続されかつ隣接する画素と接続されている。尚、コンタクトホール１５と第２バリア層８０ｂと容量線３ｂとを接続するためのコンタクトホール８ｃとが異なる平面位置に開孔することにより、コンタクトホール１５及びコンタクトホール８ｃにおける接続不良を防止することができる。

【０１３９】更に、図１４及び図１５に示すようにＴＦＴアレイ基板１０’は、配線やＴＦＴ３０の少なくとも一部が凹状に窪んで形成されており、上側表面が平坦に形成されている。この結果、データ線６ａ、走査線３ａ、容量線３ｂ等の配線やＴＦＴ３０の形成された平面領域における第３層間絶縁膜７の表面が平坦化されている。その他の構成については第１実施形態の場合と同様である。

【０１４０】従って、第４実施形態によれば、データ線６に重ねて走査線３ａ、ＴＦＴ３０、容量線３ｂ等が形成される領域との画素開口領域との段差が低減される。このようにして画素電極９ａが平坦化されているので、当該平坦化の度合いに応じて液晶層５０のディスクリネーションを低減できる。この結果、より高品位の画像表示が可能となり、画素開口領域を広げることも可能とな

る。

【０１４１】尚、このようなＴＦＴアレイ基板１０'に溝を形成することによる平坦化ではなく、例えば、ＣＭＰ（Chemical Mechanincal Polishing）処理、スピンコート処理、リフロー法等により行ったり、有機ＳＯＧ（Spin On Glass）膜、無機ＳＯＧ膜、ポリイミド膜等を利用して第２層間絶縁膜４や第３層間絶縁膜７における平坦化を行なってもよい。尚、上述の構成は第１実施形態、第２実施形態及び第３実施形態にも適用可能である。

【０１４２】（電気光学装置の全体構成）以上のように構成された各実施形態における電気光学装置の全体構成を図１６及び図１７を参照して説明する。尚、図１６は、ＴＦＴアレイ基板１０をその上に形成された各構成要素と共に対向基板２０の側から見た平面図であり、図１７は、図１６のＨ－Ｈ'断面図である。

【０１４３】図１６において、ＴＦＴアレイ基板１０の上には、シール材５２がその縁に沿って設けられており、その内側に並行して、例えば第２遮光膜２３と同じ或いは異なる材料から成る画像表示領域の周辺を規定する額縁としての第３遮光膜５３が設けられている。シール材５２の外側の領域には、データ線６ａに画像信号を所定タイミングで供給することによりデータ線６ａを駆動するデータ線駆動回路１０１及び外部回路接続端子１０２がＴＦＴアレイ基板１０の一辺に沿って設けられており、走査線３ａに走査信号を所定タイミングで供給することにより走査線３ａを駆動する走査線駆動回路１０４が、この一辺に隣接する２辺に沿って設けられている。走査線３ａに供給される走査信号遅延が問題にならないのならば、走査線駆動回路１０４は片側だけでも良いことは言うまでもない。また、データ線駆動回路１０１を画像表示領域の辺に沿って両側に配列してもよい。例えば奇数列のデータ線は画像表示領域の一方の辺に沿って配設されたデータ線駆動回路から画像信号を供給し、偶数列のデータ線は前記画像表示領域の反対側の辺に沿って配設されたデータ線駆動回路から画像信号を供給するようにしてもよい。この様にデータ線を櫛歯状に駆動するようにすれば、データ線駆動回路の占有面積を拡張することができるため、複雑な回路を構成することが可能となる。更にＴＦＴアレイ基板１０の残る一辺には、画像表示領域の両側に設けられた走査線駆動回路１０４間をつなぐための複数の配線１０５が設けられている。また、対向基板２０のコーナー部の少なくとも１箇所においては、ＴＦＴアレイ基板１０と対向基板２０との間で電気的な導通をとるための導通材１０６が設けられている。そして、図１７に示すように、図１６に示したシール材５２とほぼ同じ輪郭を持つ対向基板２０が当該シール材５２によりＴＦＴアレイ基板１０に固着されている。尚、ＴＦＴアレイ基板１０上には、これらのデータ線駆動回路１０１、走査線駆動回路１０４等に加えて、複数のデータ線６ａに画像信号を所定のタイミングで印加するサンプリング回路、複数のデータ線６ａに所定電圧レベルのプリチャージ信号を画像信号に先行して各々供給するプリチャージ回路、製造途中や出荷時の当該電気光学装置の品質、欠陥等を検査するための検査回路等を形成してもよい。尚、本実施の形態によれば、対向基板２０上の第２遮光膜２３はＴＦＴアレイ基板１０上の遮光領域よりも小さく形成すれば良く、電気光学装置の用途により、容易に取り除くことができる。

【０１４４】以上図１から図１７を参照して説明した各実施形態では、データ線駆動回路１０１及び走査線駆動回路１０４をＴＦＴアレイ基板１０の上に設ける代わりに、例えばＴＡＢ（Tape Automated bonding）基板上に実装された駆動用ＬＳＩに、ＴＦＴアレイ基板１０の周辺部に設けられた異方性導電フィルムを介して電気的及び機械的に接続するようにしてもよい。また、対向基板２０の投射光が入射する側及びＴＦＴアレイ基板１０の出射光が出射する側には各々、例えば、ＴＮ（Twisted Nematic）モード、ＶＡ（Vertically Aligned）モード、ＰＤＬＣ（Polymer Dispersed Crystal）モード等の動作モードや、ノーマリーホワイトモード／ノーマリーブラックモードの別に応じて、偏光フィルム、位相差フィルム、偏光版などが所定の方向で配置される。

【０１４５】以上説明した各実施形態における電気光学装置は、プロジェクタに適用されるため、３枚の電気光学装置がＲＧＢ用のライトバルブとして各々用いられ、各ライトバルブには各々ＲＧＢ色分解用のダイクロイックミラーを介して分解された各色の光が投射光として各々入射されることになる。従って、各実施形態では、対向基板２０に、カラーフィルタは設けられていない。しかしながら、第２遮光膜２３の形成されていない画素電極９ａに対向する所定領域にＲＧＢのカラーフィルタをその保護膜と共に、対向基板２０上に形成してもよい。このようにすれば、液晶プロジェクタ以外の直視型や反射型のカラー電気光学装置に各実施形態における電気光学装置を適用できる。更に、対向基板２０上に１画素１個対応するようにマイクロレンズを形成してもよい。あるいは、ＴＦＴアレイ基板１０上のＲＧＢに対向する画素電極９ａ下にカラーレジスト等でカラーフィルタ層を形成することも可能である。このようにすれば、入射光の集光効率を向上することで、明るい電気光学装置が実現できる。更にまた、対向基板２０上に、何層もの屈折率の相違する干渉層を堆積することで、光の干渉を利用して、ＲＧＢ色を作り出すダイクロイックフィルタを形成してもよい。このダイクロイツクフィルタ付き対向基板によれば、より明るいカラー電気光学装置が実現できる。

【０１４６】以上説明した各実施形態における電気光学装置では、従来と同様に入射光を対向基板２０の側から入射することとしたが、第１遮光膜１１ａ（あるいは１

１ａ’）を設けているので、ＴＦＴアレイ基板１０の側から入射光を入射し、対向基坂２０の側から出射するようにしても良い。即ち、このように電気光学装置をプロジェクタに取り付けても、半導体層１ａのチャネル領域１ａ’及び低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃに光が入射することを防ぐことが出来、高画質の画像を表示することが可能である。ここで、従来は、ＴＦＴアレイ基板１０の裏面側での反射を防止するために、反射防止用のＡＲ（Anti Reflection）被膜された偏光板を別途配置したり、ＡＲフィルムを貼り付ける必要があったが、各実施形態では、ＴＦＴアレイ基板１０の表面と半導体層１ａの少なくともチャネル領域１ａ’及び低濃度ソース領域１ｂ及び低濃度ドレイン領域１ｃとの間に第１遮光膜１１ａ（あるいは１１ａ’）が形成されているため、このようなＡＲ被膜された偏光板やＡＲフィルムを用いたり、ＴＦＴアレイ基板１０そのものをＡＲ処理した基板を使用する必要が無くなる。従って、各実施形態によれば、材料コストを削減でき、また偏光板貼り付け時に、ごみ、傷等により、歩留まりを落とすことがなく大変有利である。また、耐光性が優れているため、明るい光源を使用したり、偏光ビームスプリッタにより偏光変換して、光利用効率を向上させても、光によるクロストーク等の画質劣化を生じない。

【０１４７】また、各画素に設けられるスイッチング素子としては、正スタガ型又はコプラナー型のポリシリコンＴＦＴであるとして説明したが、逆スタガ型のＴＦＴやアモルファスシリコンＴＦＴ等の他の形式のＴＦＴに対しても、各実施形態は有効である。

【０１４８】（電子機器）次に、以上詳細に説明した電気光学装置１００を備えた電子機器の実施の形態について図１８から図２０を参照して説明する。

【０１４９】先ず図１８に、このように電気光学装置１００を備えた電子機器の概略構成を示す。

【０１５０】図１８において、電子機器は、表示情報出力源１０００、表示情報処理回路１００２、駆動回路１００４、電気光学装置１００、クロック発生回路１００８並びに電源回路１０１０を備えて構成されている。表示情報出力源１０００は、ＲＯＭ（Read Only Memory）、ＲＡＭ（Random Access Memory）、光ディスク装置などのメモリ、画像信号を同調して出力する同調回路等を含み、クロック発生回路１００８からのクロック信号に基づいて、所定フォーマットの画像信号などの表示情報を表示情報処理回路１００２に出力する。表示情報処理回路１００２は、増幅・極性反転回路、シリアルーパラレル変換回路、ローテーション回路、ガンマ補正回路、クランプ回路等の周知の各種処理回路を含んで構成されており、クロック信号に基づいて入力された表示情報からデジタル信号を順次生成し、クロック信号ＣＬＸと共に駆動回路１００４に出力する。駆動回路１００４は、電気光学装置１００を駆動する。電源回路１０１０は、上述の各回路に所定電源を供給する。尚、電気光学装置１００を構成するＴＦＴアレイ基板の上に、駆動回路１００４を搭載してもよく、これに加えて表示情報処理回路１００２を搭載してもよい。

【０１５１】次に図１９から図２０に、このように構成された電子機器の具体例を各々示す。

【０１５２】図１９において、電子機器の一例たるプロジェクタ１１００は、上述した駆動回路１００４がＴＦＴアレイ基板上に搭載された電気光学装置１００を含むライトバルブを３個用意し、各々ＲＧＢ用のライトバルブ１００Ｒ、１００Ｇ及び１００Ｂとして用いたプロジェクタとして構成されている。プロジェクタ１１００では、メタルハライドランプ等の白色光源のランプユニット１１０２から投射光が発せられると、３枚のミラー１１０６及び２枚のダイクロイツクミラー１１０８によって、ＲＧＢの３原色に対応する光成分Ｒ、Ｇ、Ｂに分けられ、各色に対応するライトバルブ１００Ｒ、１００Ｇ及び１００Ｂに各々導かれる。この際特にＢ光は、長い光路による光損失を防ぐために、入射レンズ１１２２、リレーレンズ１１２３及び出射レンズ１１２４からなるリレーレンズ系１１２１を介して導かれる。そして、ライトバルブ１００Ｒ、１００Ｇ及び１００Ｂにより各々変調された３原色に対応する光成分は、ダイクロイックプリズム１１１２により再度合成された後、投射レンズ１１１４を介してスクリーン１１２０にカラー画像として投射される。

【０１５３】図２０において、電子機器の他の例たるマルチメディア対応のラップトップ型のパーソナルコンピュータ（ＰＣ）１２００は、上述した電気光学装置１００がトップカバーケース内に設けられており、更にＣＰＵ、メモリ、モデム等を収容すると共にキーボード１２０２が組み込まれた本体１２０４を備えている。

【０１５４】以上図１９から図２０を参照して説明した電子機器の他にも、液晶テレビ、ビューファインダ型又はモニタ直視型のビデオテープレコーダ、カーナビゲーション装置、電子手帳、電卓、ワードプロセッサ、エンジニアリング・ワークステーション（ＥＷＳ）、携帯電話、テレビ電話、ＰＯＳ端末、タッチパネルを備えた装置等などが図１８に示した電子機器の例として挙げられる。

【０１５５】以上説明したように、本実施の形態によれば、製造効率が高く高品位の画像表示が可能な電気光学装置を備えた各種の電子機器を実現できる。

【図面の簡単な説明】

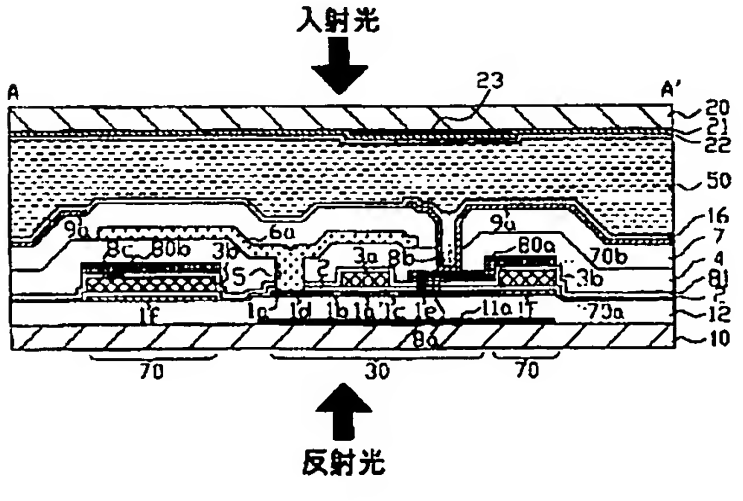
【図１】第１実施形態の電気光学装置における画像表示領域を構成するマトリクス状の複数の画素に設けられた各種素子、配線等の等価回路である。

【図２】第１実施形態の電気光学装置におけるデータ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図である。

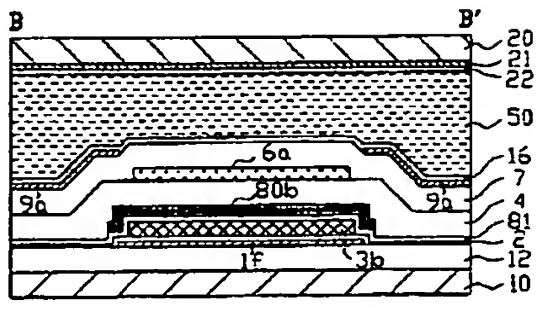
【図３】図２のＡ－Ａ’断面図である。
【図４】図２のＢ－Ｂ’断面図である。
【図５】第１実施形態の電気光学装置の製造プロセスを順を追って示す工程図（その１）である。
【図６】第１実施形態の電気光学装置の製造プロセスを順を追って示す工程図（その２）である。
【図７】第１実施形態の電気光学装置の製造プロセスを順を追って示す工程図（その３）である。
【図８】第１実施形態の電気光学装置の製造プロセスを順を追って示す工程図（その４）である。
【図９】第２実施形態の電気光学装置におけるデータ線、走査線、画素電極等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図である。
【図１０】図１０のＡ－Ａ’断面図である。
【図１１】図１０のＢ－Ｂ’断面図である。
【図１２】第３実施形態の電気光学装置の断面図である。
【図１３】第４実施形態の電気光学装置におけるデータ線、走査線、画素電極、遮光膜等が形成されたＴＦＴアレイ基板の相隣接する複数の画素群の平面図である。
【図１４】図１３のＡ－Ａ’断面図である。
【図１５】図１３のＢ－Ｂ’断面図である。
【図１６】各実施形態の電気光学装置におけるＴＦＴアレイ基板をその上に形成された各構成要素と共に対向基板の側から見た平面図である。
【図１７】図１６のＨ－Ｈ’断面図である。
【図１８】本発明による電子機器の実施の形態の概略構成を示すブロック図である。
【図１９】電子機器の一例としてプロジェクタを示す断面図である。
【図２０】電子機器の他の例としてのパーソナルコンピュータを示す正面図である。
【符号の説明】
１ａ…半導体層
１ａ’…チヤネル領域
１ｂ…低濃度ソース領域

１ｃ…低濃度ドレイン領域
１ｄ…高濃度ソース領域
１ｅ…高濃度ドレイン領域
１ｆ…第１蓄積容量電極
２…絶縁薄膜
３ａ…走査線
３ｂ…容量線
４…第２層間絶縁膜
５…コンタクトホール
６ａ…データ線
６ｂ…中継導電層
７…第３層間絶縁膜
８ａ…コンタクトホール
８ｂ…コンタクトホール
９ａ…画素電極
１０…ＴＦＴアレイ基板
１１ａ…第１遮光膜
１２…下地絶縁膜
１６…配向膜
２０…対向基板
２１…対向電極
２２…配向膜
２３…第２遮光膜
３０…ＴＦＴ
５０…液晶層
７０…蓄積容量
７０ａ…第１蓄積容量
７０ｂ…第２蓄積容量
８０ａ…第１バリア層
８０ｂ…第２バリア層
８１…第１層間絶縁膜
８８ａ…コンタクトホール
８８ｂ…コンタクトホール
８８ｃ…コンタクトホール
８８ｄ・・・コンタクトホール

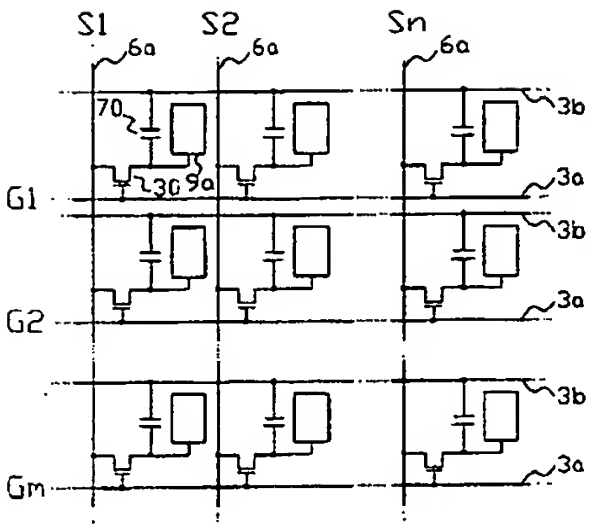
【図３】



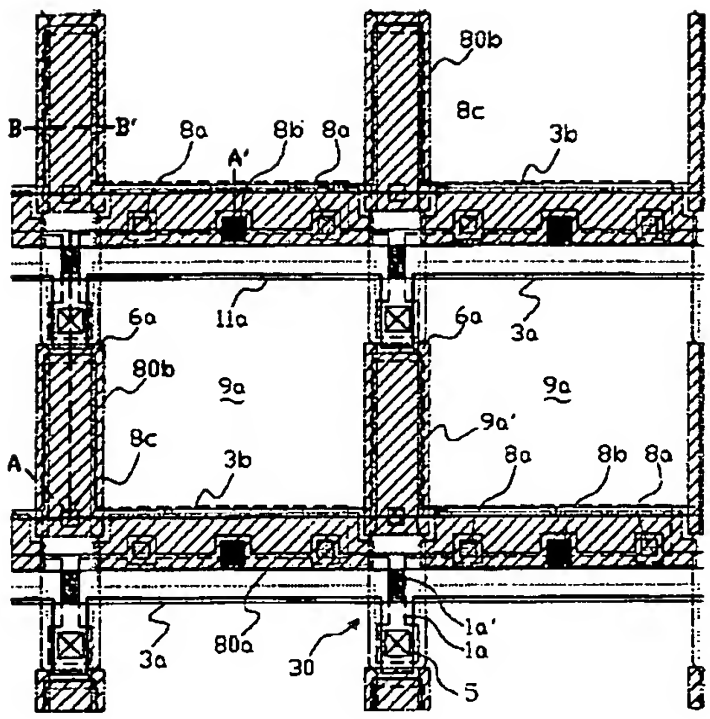
【図４】



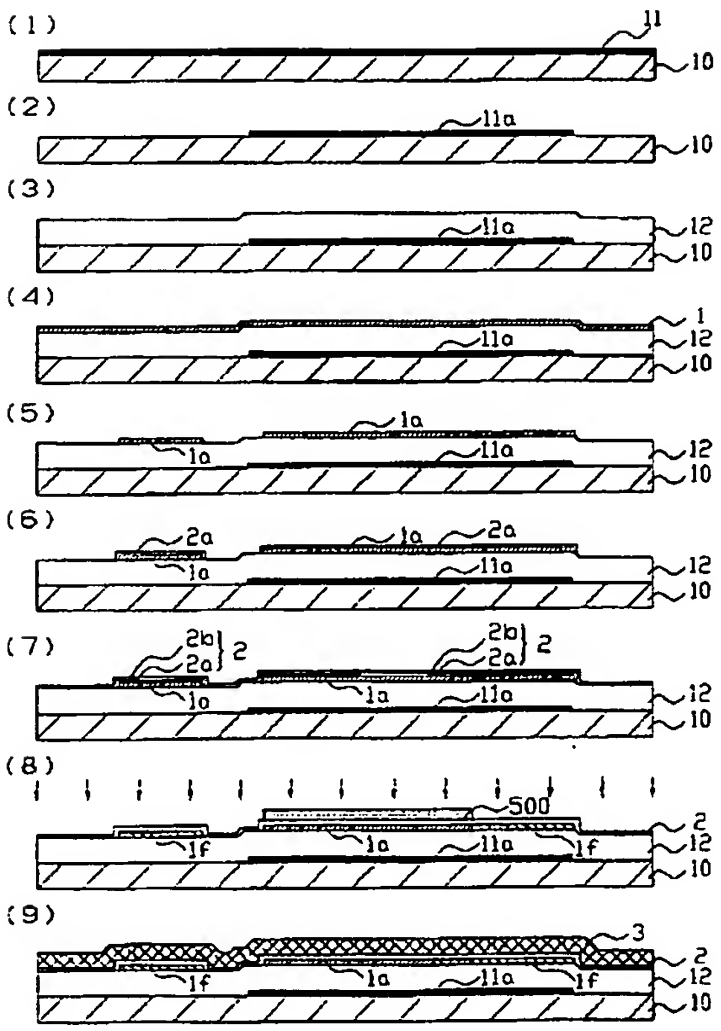
【図１】


S1
S2
Sn
6a
70
30
9a
3b
3a
G1
G2
Gm

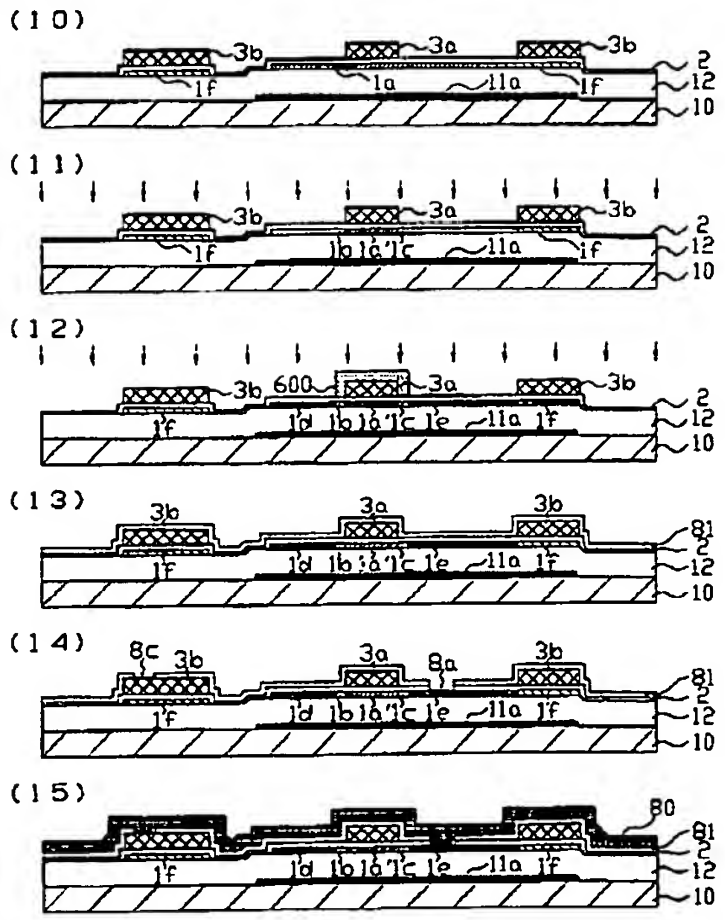
【図２】


80b
8c
B
B'
8a
8b
A'
3b
6a
11a
3a
9a
9a'
A
1a'
1a
30
5
80a

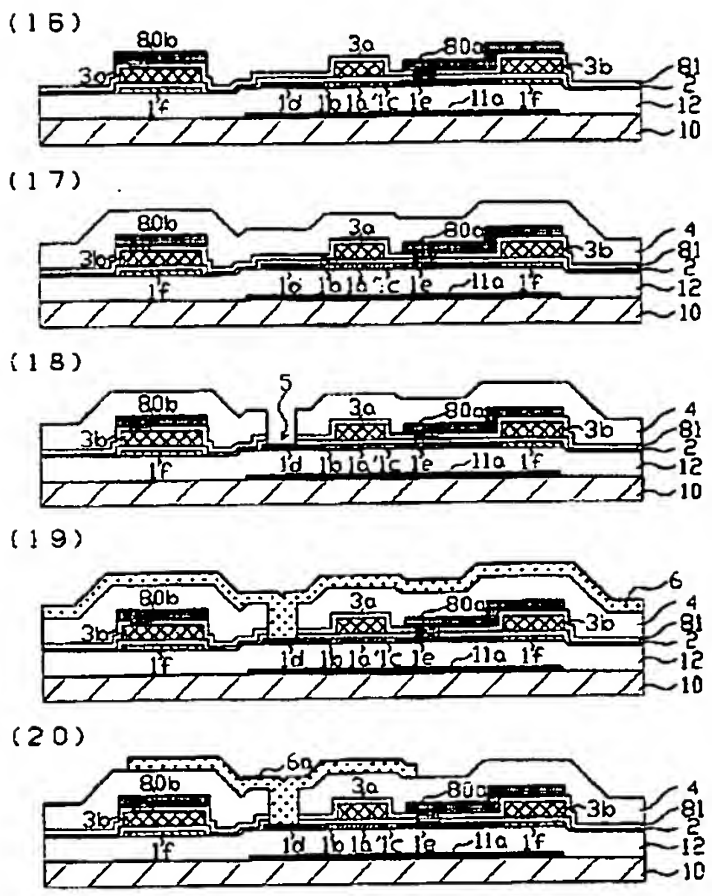
【図５】


(1)
11
10
(2)
11a
(3)
12
(4)
1
(5)
1a
(6)
2a
(7)
2b
2
(8)
500
1f
(9)
3

【図６】


(10)
3b
3a
2
12
10
(11)
(12)
600
(13)
81
(14)
8c
8a
(15)
80

【図７】



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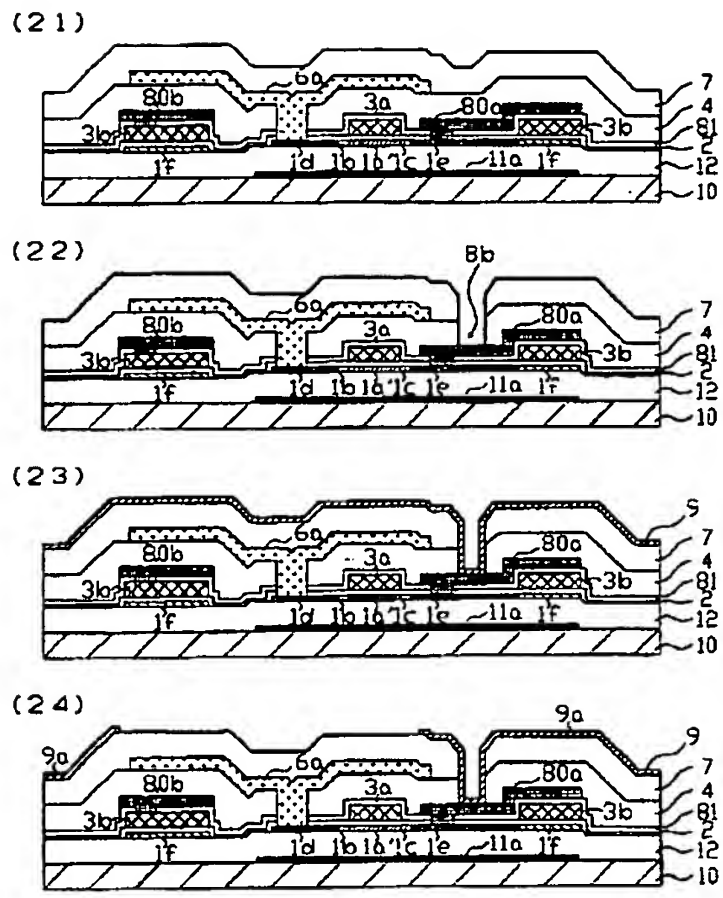

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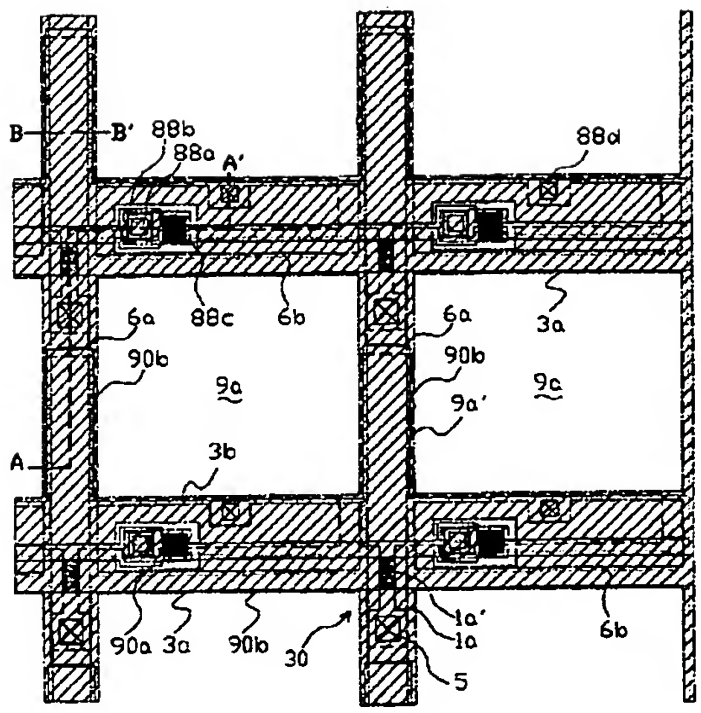

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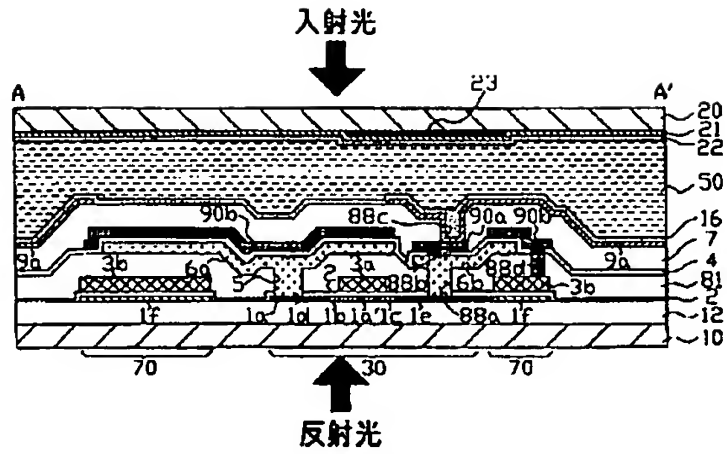
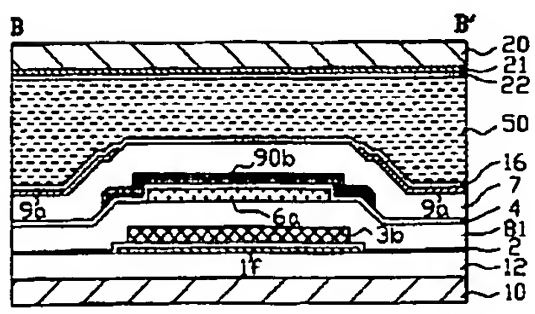


【図１１】



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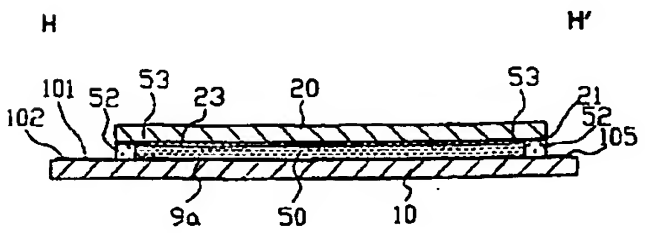

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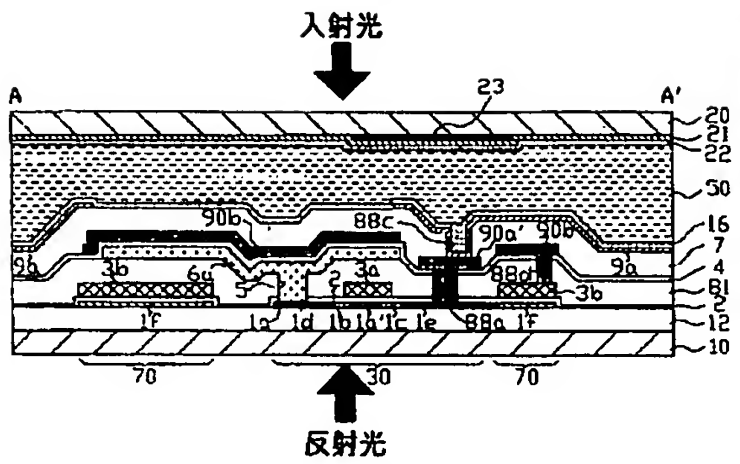

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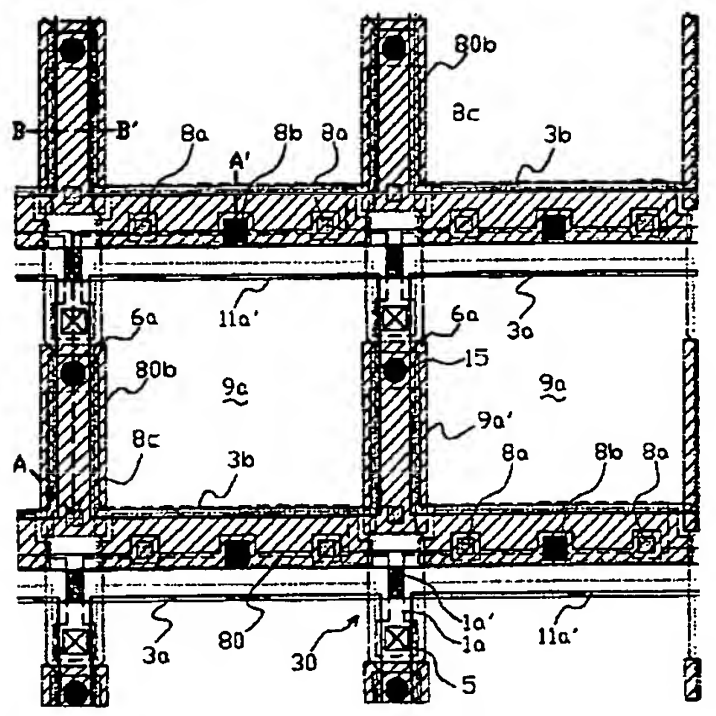

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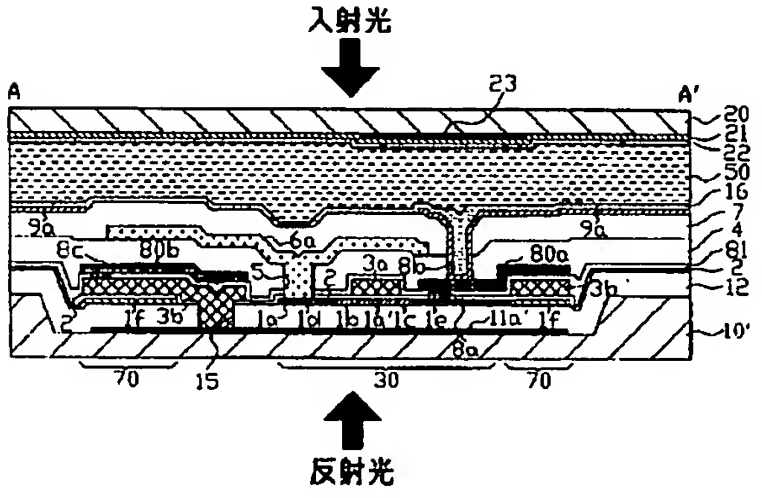

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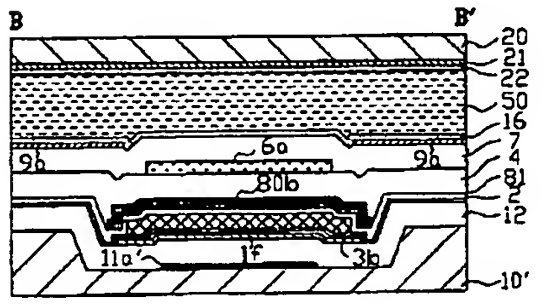

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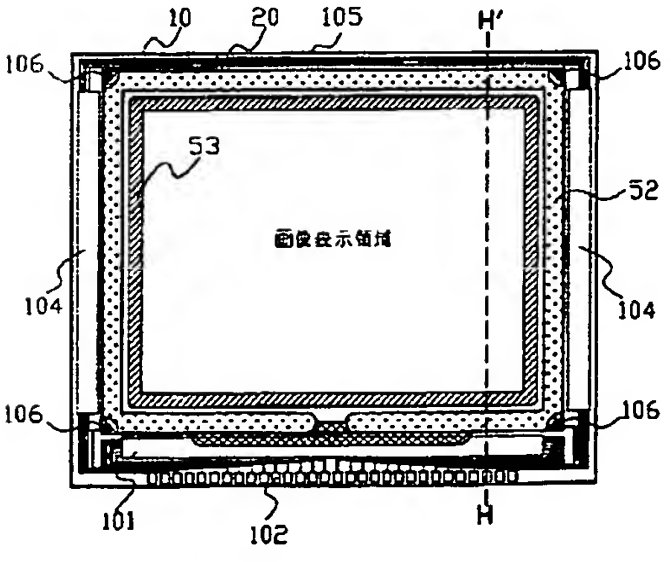

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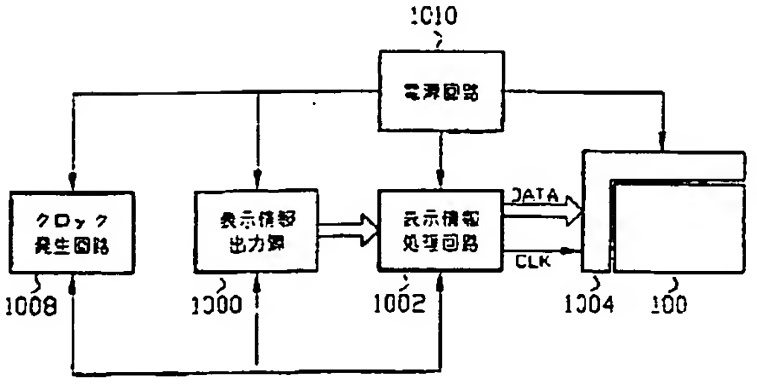

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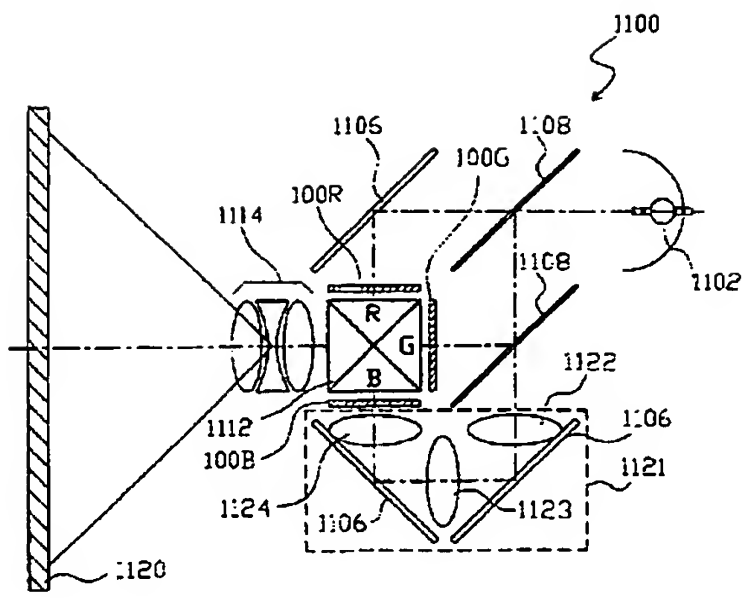
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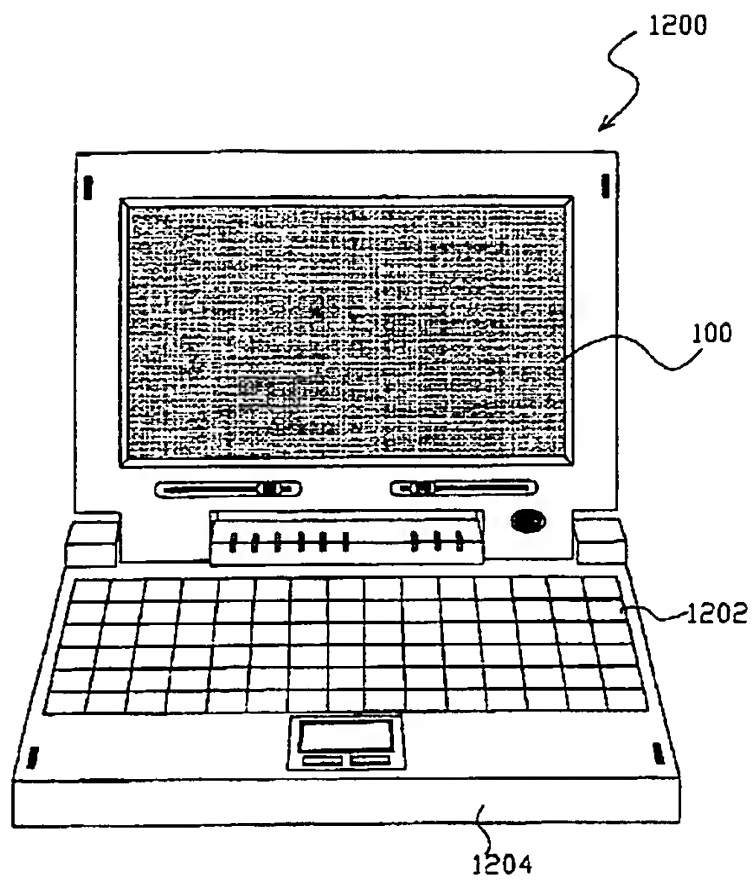
1123
1120

【図２０】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FF02 FF03 FF09 FF23 FF30
FF32 GG02 GG13 GG25 GG32
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